When this manual was scanned in June 2024 some errors and omissions were noticed.

The same photograph of the instrument's controls appears several times in the printed manual
to make the accompanying text more readable. This feature has been retained in the pdf.

The page numbers in the contents page are incomplete and/or incorrect.

There are duplicate pages 19 & 20.

The real page 19 starts midway through a line and seems to be the end of para 4.3. Para 4.2 and 4.3 are missing.

19 is probably the start of section 5 and could be page 31 with pages 32 & 33 missing. I have named this "31"

20 is probably start of section 6 and has been inserted there.

POST OFFICE OSCILLOSCOPE No.18A

Instruction Manual

GOULD

Hainault Essex England

Telephone 01-500 1000
Telegrams Attenuate Ilford
Telex 263785

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N.B. Components shown only in servicing manual.

Amendments

Paragraph 3.17. Last sentence should read: e.g. If 2V is selected on the video input attenuator then the peak-to-peak amplitude of the calibration waveform c.r.t. display corresponds to 2V signal input at "VIDEO IN".

Introduction

Section 1

Oscilloscope No. 18A includes a dual-trace single time-base facility with triggering from one of two Signal inputs. The main input ("VIDEO IN") is 75Ω impedance and offers comprehensive video triggering for the examination of line repetitive and I.T.S. television signals. The coax link between the VIDEO OUT and CH2 INPUT sockets is a permanent connection for this mode of operation.

The second input ('CH1') is high impedance and is intended to complement the 'VIDEO IN' input when measuring Differential Phase and Gain, Random Noise, Hum and Non Linearity distortions.

See P.O. Drawing 400455 for full details of connections and tests to be made.

When using the VIDEO INPUT, a black level clamp may be applied to the signal and the timebase used to give detailed examination of 625 line television waveforms or to display a picture. It accepts a standard level video signal, and provides the following trigger modes. Field 1 or 2 or both fields alternating, line repetitive, l.e.d. identification of any one selected line and line pairs in the range 16/329 to 22/335 inclusive. The triggering may be delayed continuously up to 80μs allowing detailed examination of any part of the line. When displaying a television picture the triggering point selected is indicated by a 'bright-up' on the picture. To provide maximum brightness on all TV waveforms likely to be encountered, the c.r.t. is operated at an overall voltage of 16kV. To protect the c.r.t. screen from excessive beam current at low scan rates, an automatic beam current limiting circuit has been included. It should be noted that shading of the c.r.t. display may occur if the trace intensity is increased excessively, whilst operating at slow scan rates. This is not a fault, but simply the correct operation of the beam current limiting circuit. Under such circumstances, reducing the trace intensity to a more convenient viewing level will remove this effect.

The Oscilloscope No. 18A is derived from a commercially available instrument and so includes several features unnecessary for Post Office use. However for general interest a description of these features also has been included in this manual.

N.B. In the VIDEO INPUT mode particular care must be taken to ensure the correct use of the 3 position input attenuator in conjunction with the variable and switched Y gain controls of CH2, as mis-operation can introduce errors. See Paragraphs 3.9 and 3.4.



Portable Version



Rack mount version

Short Form

Specification

Section 2

(For Full Description see Contractual Documents)

DISPLAY

CRT 8 x 10cm Rectangular
EHT 16kV overall
Geometry Horizontal Trace flatness shall not exceed ±0.25mm deviation, 30mm either side of the c.r.t. centre.
Phosphor P31 standard, P7 option.
Beam Finder Compresses trace to within graticule area regardless of settings of the vertical and horizontal position controls.

VERTICAL DEFLECTION

Display Modes CH1 only
CH2 only
Channel CH1 and CH2 chopped (500kHz approx.)
CH1 and CH2 alternate
CH1 ± CH2 (Algebraic addition)

CH1 INPUT

Bandwidth DC 10MHz (−3dB) DC coupled. 2Hz − 10MHz (−3dB) AC coupled.
Rise Time 35ns.
Input Coupling DC − Ground − AC.
Deflection Coefficient 5mV/cm to 20V/cm in 1-2-5 sequence, with uncalibrated fine gain control giving 2.5:1 reduction in sensitivity. Warning Light indicates uncalibrated setting. A x 5 facility on CH1 gives maximum sensitivity of 1mV/cm.
Accuracy ± 3% (± 5% on x5).
Input Impedance 1MΩ/28pF
Max. Input Voltage 400V (DC plus pk AC).

VIDEO INPUT

(CH2, non inverted mode). (Signal transfer from Video Output to CH2 Y-Input).
Video Waveform Accepts European PAL 625 line video composite sync which may contain 'sound-in-sync' pulses. Positive-going video, negative-going sync. (Peak white video to sync ratio 0.7:0.3 nominal.)
Amplitude/Frequency Response Decreases steadily from DC (2Hz) up to and beyond 3dB cut-off frequency.
Bandwidth Relative to 50kHz. Less than 0.3dB, 1dB and 3dB at 10MHz, 20MHz and 32MHz respectively. Response at 4.43MHz within 0.1dB of level at 10kHz.
Input Impedance 75 ohms ± 1%.
Video Sensitivity With 5:1 variable at centre position, 50mm picture height (excluding sync) display for 1V peak-to-peak input at X1 gain and 1V input attenuator setting.
Input Attenuator 3-position lever switch
Upper Position +6dB (2V range)
Centre Position 0dB (1V range)
Lower Position −6dB (0.5V range)
Attenuator Accuracy ±0.05dB on +6dB and -6dB. positions relative to the 0dB range.
Gain Selection X1 or X2 switched gain with uncalibrated fine gain control giving 2.5:1 reduction in sensitivity for full TV performance.
Position Control Coarse and fine control with 5:1 reduction.
Minimum Video Signal 0.125V p-p when using 0.5V range (12dB below nominal of each range).
Maximum Video Signal 6V p-p when using 2V range (12dB above nominal level of each range).
Maximum Sustained Input 4V rms.
Maximum Acceptable Noise with respect to Peak Luminance Amplitude −30dB for white noise (0−6MHz) unweighted. r.m.s.
'Clamp out' Direct through coupling.
'Clamp' Video black level held to 0V ± 10mV with no input signal. Hum rejection nominally 20dB min.
Transfer Sensitivity Matching 'Clamp' to 'Clamp Out' ±0.1dB.

Display Modes:
'Picture' Provides a Z-modulated picture via 625 line raster on crt, size approximately 8cm wide by 6.5cm high. Selected line and delay position is shown intensified.

'Line Pairs'	16 and 329	Lines Overlaid. Trigger point occurs before leading edges of sync pulses on selected lines.
	17 and 330	
	18 and 331	
	19 and 332	
	20 and 333	
	21 and 334	
	22 and 335	

TV Field:

'Both'	Trigger point occurs just after
'Odd'	first broad pulse
'Even Fields'	

'Line Repetitive' Trigger occurs before leading edges of syncs on alternate lines.
'Line Selector' Any of 625 lines may be selected. Line chosen shown by LED display. Line number may be advanced or retarded using 'UP' or 'Down' push buttons. Trigger occurs before leading edge of sync pulse.
'Calibrator'

1) Internal − replaces video display with two parallel lines for VOLTS−CAL procedure on "VIDEO IN" channel. Accuracy ±0.5%.
2) External − 1V peak-peak output ± 1% on front panel pin.
   Calibrator frequency 1kHz ± 5%.

Waveform Response: Sin^{-2} Pulse and Bar:
25μs Bar ⩽ 0.5%k
2T Pulse ⩽ 0.25%k
T Pulse overshoot ⩽ 0.5%
L.F. response (50Hz square wave) ⩽ 0.25%k

Clamped Response: As above but relaxed by a factor of two. All waveform performance figures confirmed at X 2 gain (i.e. 100mm picture height).

Specification

Section 2

HORIZONTAL DEFLECTION

Time Base:

Time Coefficients 100ns/cm to 1s/cm in 22 steps (1-2-5 sequence).

An uncalibrated fine control reduces sweep rate by 2.5 times (slowest sweep rate approx. 0.5min). A warning light indicates uncalibrated settings.

Max. Sweep Rate x5 X-expansion gives max. sweep rate of 20ns/cm.

Accuracy ±3% (±5% on x5).

Triggering:

Source Internal CH1 pos. or neg. slope
Internal CH2 pos. or neg. slope
External, pos. or neg. slope
Mains Lock, pos. or neg. slope
TV
TV overlay
Free run

Input Coupling AC [TV], AC HF, AC LF [50Hz], DC.

External Trigger Input impedance 100k in parallel with 10pF.

Modes

Manual level
Bright line auto (40Hz to 5MHz)
TV. Triggering occurs on TV waveforms at points described in section covering 'Video Input Display Modes',

Sensitivity

Internal:	Manual –	2mm to 5MHz
		1cm at 50MHz
Auto:	3mm to 2MHz	
TV:	0.125V p-p signal	
External:	Manual –	300mV to 5MHz
		1.5V at 50MHz
Auto:	500mV at 2MHz	

Delay (TV only) Delays start of sweep from approx. 10μs to 80μs adjustable by 10 turn control.

Delay Jitter <10ns.

Horizontal Amplifier (rear panel):

Bandwidth DC – 2 MHz (3dB)

Deflection Coefficient 1V/cm. The x5 X-expansion facility increases sensitivity to 0.2V/cm.

Input Impedance 100k ohms.

X-Y Operation With CH2 output (rear panel) coupled to Ext. X input and x5 X-expansion selected:-
Bandwidth DC–1MHz; Phase shift <3° at 50kHz:
Sensitivity as CH2 input attenuator, divided by two.

Z-Modulation (rear panel):

Bandwidth D.C. – 10 MHz

Sensitivity +1V for visible modulation at low intensity. +20V for blanking from normal intensity.

Input Impedance 47k ohms.

OUTPUTS

Front Panel:

Calibrator See under 'Video Input Display Modes'.

Trigger (Video) Provides a square wave output (approx. 0–4V with output impedance of approx. 10k ohms). Positive leading edge corresponds to undelayed trigger, trailing edge to delayed trigger.

Sync (Video) Provides negative-going composite sync from approx. +5V to zero, with an output impedance of approx. 10k ohms.

Rear Panel:

Normal Timebase Ramp From 10k ohms source, output via 4mm socket.

CH2 Output Output 100mV per cm deflection, via BNC socket.

'Picture Output' Normally linked to 'Z Mod' input.

SUPPLIES

Input Voltage 95–111V, 103–121V, 111–130V, 190–222V, 206–242V, 222–260V.

Frequency 45 – 440Hz

Consumption 70VA approx.

OPERATING TEMPERATURE RANGE

0 to +50°C

Full specification is met over range +15°C to +35°C.

SIZE AND WEIGHT Portable Version

7" (18cm) x 11⅜" (29cm) x 16½" (42cm)

27 lbs (12kg)

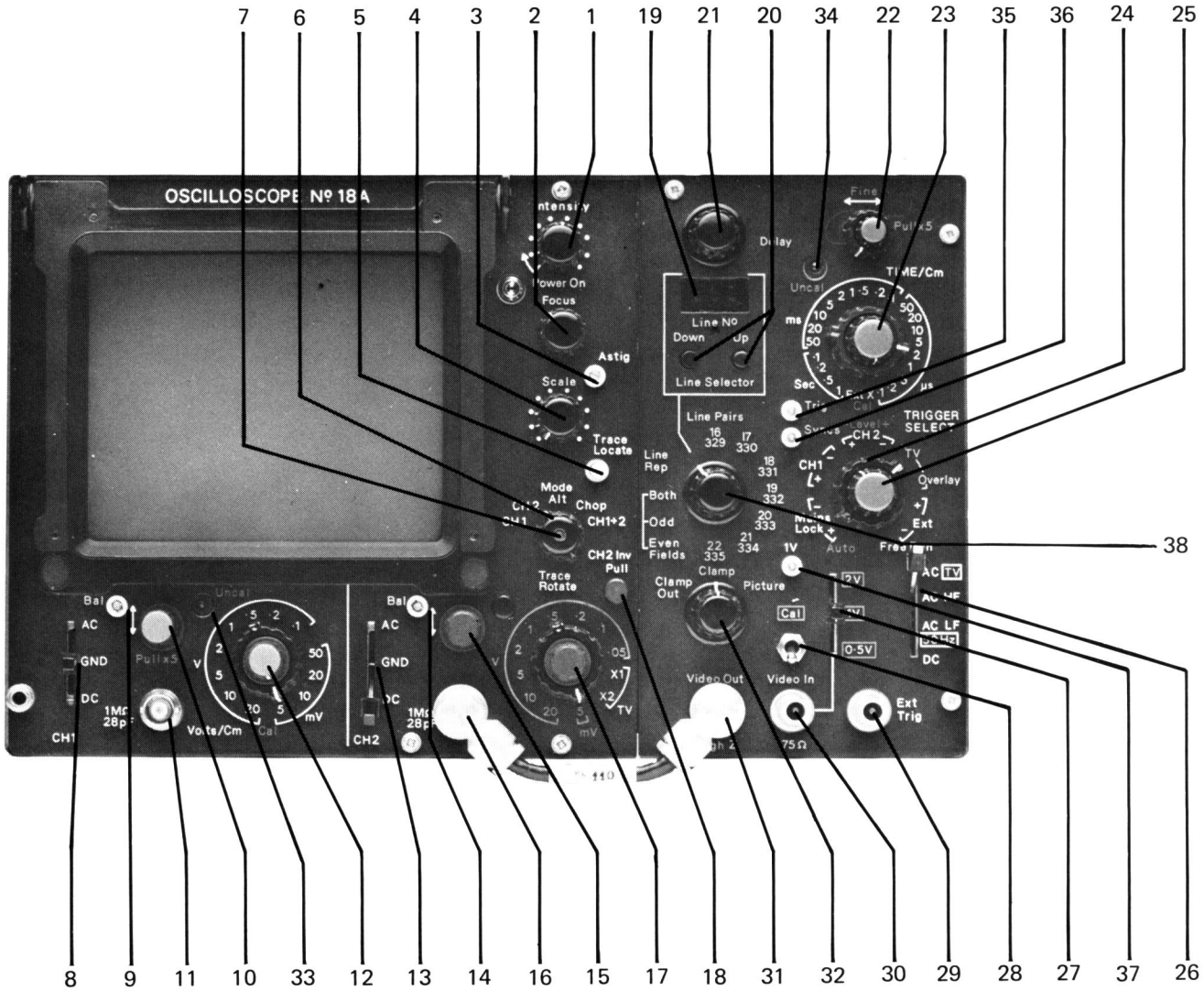
Rack Mounting Version

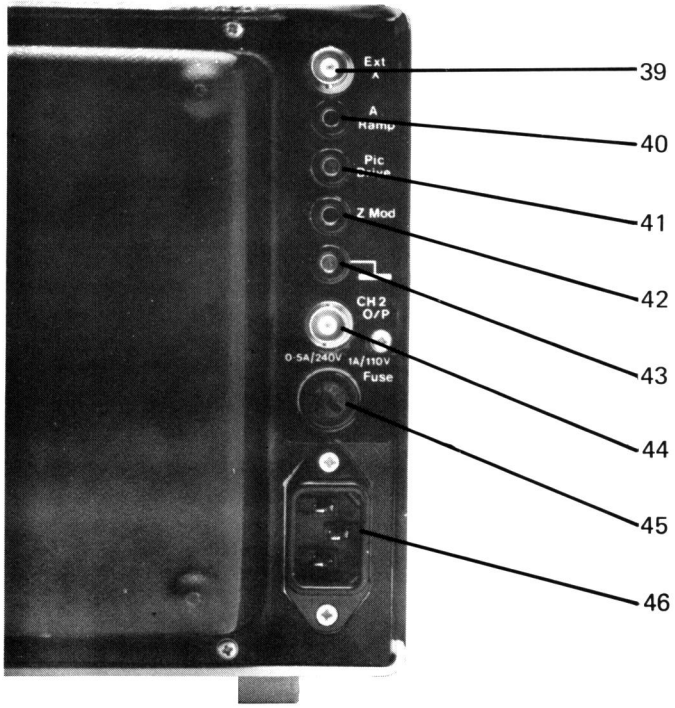
Fits standard 19" rack, otherwise as per portable version.

ACCESSORIES SUPPLIED

Handbook P/No. 32262

1 off BNC-Clips lead	PL44
2 off 4mm plug	PN1244
1 off TNC-TNC lead	PL110
1 off Link (Video O/P-Z mod) P/No. 40671	PL106
1 off supply lead	PL94


7 6 5 4 3 2 1 19 21 20 34 22 23 35 36 24 25
OSCILLOSCOPE Nº 18A
Intensity
Power On
Focus
Astig
Scale
Trace Locate
Mode
Alt
Chop
CH1+2
CH2 Inv
Pull
Trace Rotate
Delay
Fine
Pull x5
Uncal
TIME/Cm
Line Nº
Down
Up
Line Selector
Line Pairs
16 329
17 330
18 331
19 332
20 333
21 334
22 335
Line Rep
Both
Odd
Even Fields
Clamp
Clamp Out
Picture
Cal
Video Out
Video In
75Ω
TRIGGER SELECT
CH1
CH2
TV
Overlay
Ext
Auto
Lock
1V
2V
5V
0·5V
AC TV
AC HF
AC LF
DC
Ext Trig
Bal
AC
GND
DC
1MΩ 28pF
Pull x5
Volts/Cm
Cal
mV
X1
X2
38
8 9 11 10 33 12 13 14 16 15 17 18 31 32 30 29 28 27 37 26


Ext A
A Ramp
Pic
Z Mod
CH2 O/P
0·5A/240V
1A/110V
Fuse
39
40
41
42
43
44
45
46

Operation

Section 3

3.1 CONNECTORS AND CONTROLS

FRONT PANEL

(1) POWER ON/INTENSITY: Switches instrument on and varies brightness of c.r.t. display.

(2) FOCUS: Provides adjustment to give the smallest spot or finest trace.

(3) ASTIG: Provides adjustment of the c.r.t. spot shape.

(4) SCALE: Controls graticule illumination.

(5) TRACE LOCATE: Locates trace when depressed if trace not in view on c.r.t. display.

(6) MODE SWITCH: A five position rotary switch enabling the following selection of 1/P channels to be displayed.

CHANNEL 1 ONLY
CHANNEL 2 ONLY
CHANNEL 1 AND CHANNEL 2 CHOPPED
CHANNEL 1 AND CHANNEL 2 ALTERNATE
CHANNEL 1 PLUS CHANNEL 2 (ALGEBRAIC ADDITION)

(7) TRACE ROTATE: Enables trace to be aligned horizontally with graticule.

(8)(13) INPUT CONDITION: AC/GND/DC. A three position toggle switch which selects ac, dc or grounded signal coupling.

(9)(14) BAL.: Balance control adjusted to eliminate trace movement when the variable gain is altered.

(10) ↕ CHANNEL 1 SHIFT giving vertical control of trace position.

PULL x 5 Mag A push pull switch which increases gain of CHANNEL 1 five times.

(11)(16) CHANNEL 1 AND CHANNEL 2 INPUT SOCKETS. Input impedance 1MΩ/28pF.

(12) VOLTS/CM: A twelve position rotary switch which selects the deflection factor of Channel 1 with fine control giving 2.5 : 1 reduction in sensitivity.

(15) ↕ CHANNEL 2 SHIFT with reduction gearing to give fine control of vertical position.

(17) VOLTS/CM: A twelve position rotary switch which selects the deflection factor of Channel 2 with uncalibrated 5 turn fine gain control.

(18) CH2 INV. Pull switch inverts the normal display on 'VIDEO IN' channel.

(19) LINE NO: 3 digit L.E.D. display indicating line number selected.

(20) LINE SELECTOR: 2 push buttons enable counting up and down for line by line examination of 625 line television waveforms.

(21) DELAY: This control enables TV triggering to be delayed by up to at least 80μsec.

(22) FINE ◄► PULL x 5 Pulling centre knob out increases gain of X amplifier five times. Any portion of sweep length may be viewed by adjusting coarse (◄►) or FINE shift controls.

(23) TIME/CM: This is a 23 position switch which provides control of the timebase velocity from 0.1μs/cm to 1 sec/cm. The steps are only calibrated when the concentric variable control is in the fully clockwork position (CAL). In addition to selection of the speed of the internal timebase the switch has a functional setting EXT X in which the internal timebase is inoperative.

(24) This is the TRIGGER SELECT switch which is set to the required trigger source.

CH1 ± Internal Channel 1 positive or negative slope

CH2 ± Internal Channel 2 positive or negative slope

MAINSLOCK ± 50c/s Mains supply positive or negative slope

EXT ± External trigger source positive or negative slope

TV Correct trigger setting for TV input signals (except 50Hz on line synce test waveform when CH2 ± trigger select should be used), also introduces TV trigger 'Delay' facility (21).

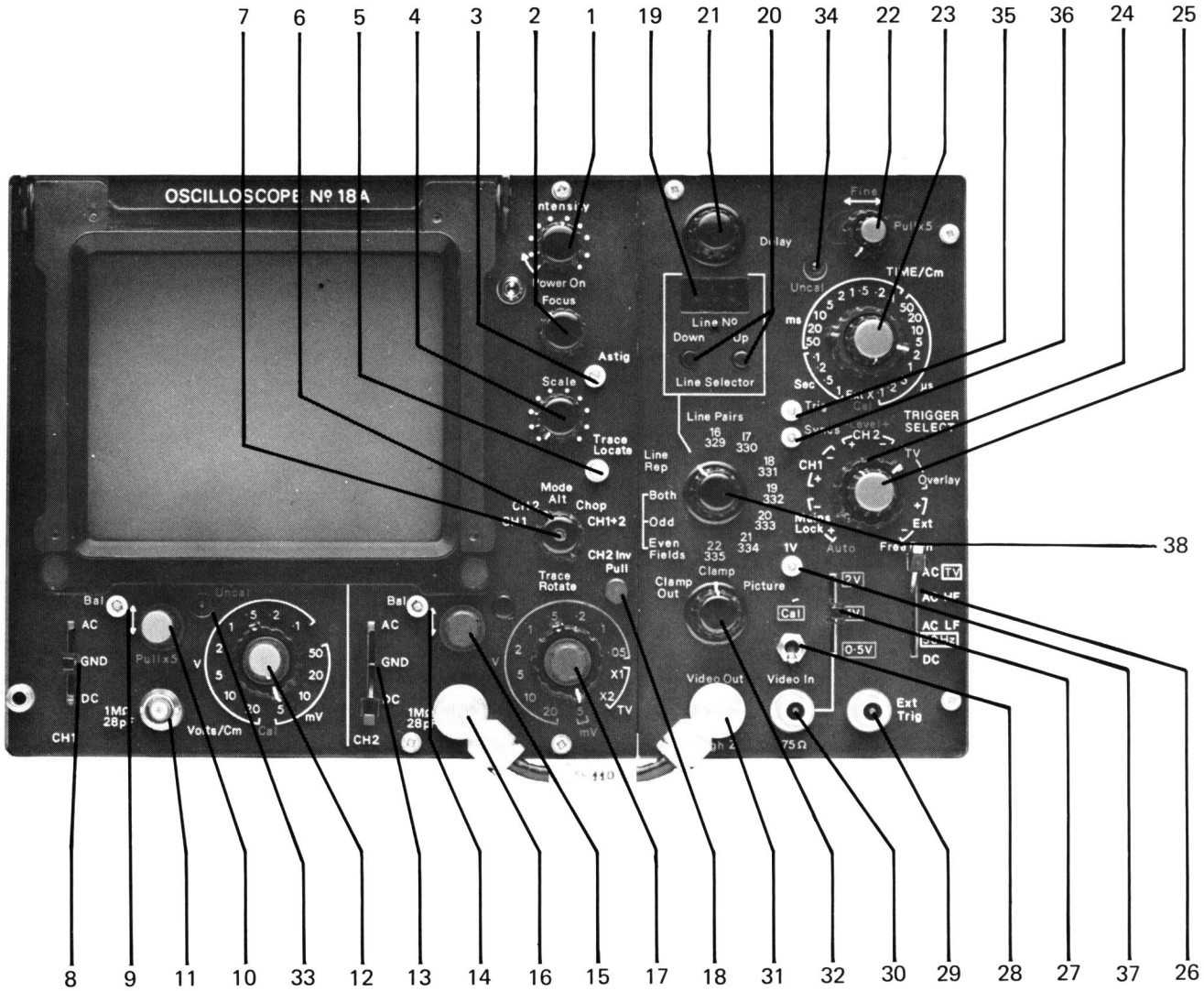
OVERLAY As above, but retriggers timebase to provide TV line overlay.

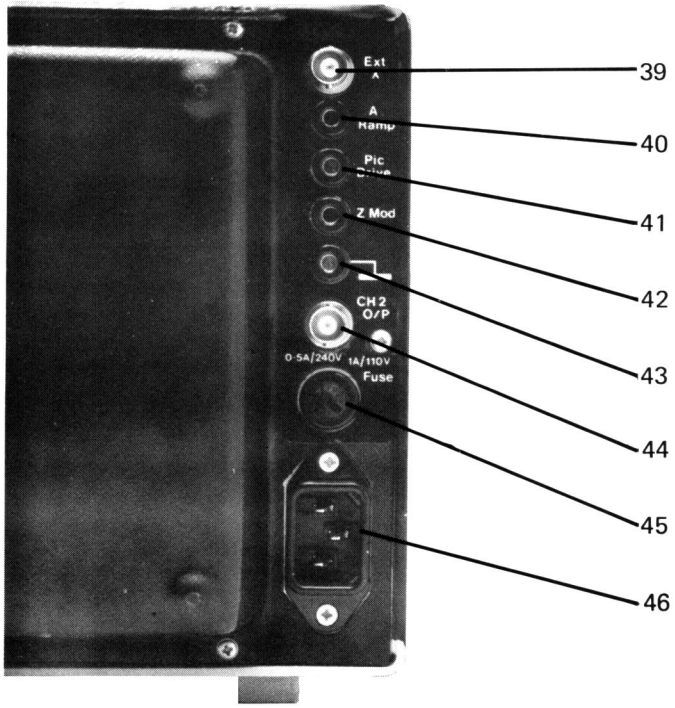
(25) LEVEL: This control is concentric with the Trigger mode switch and allows selection of the triggering point on the trigger waveform.

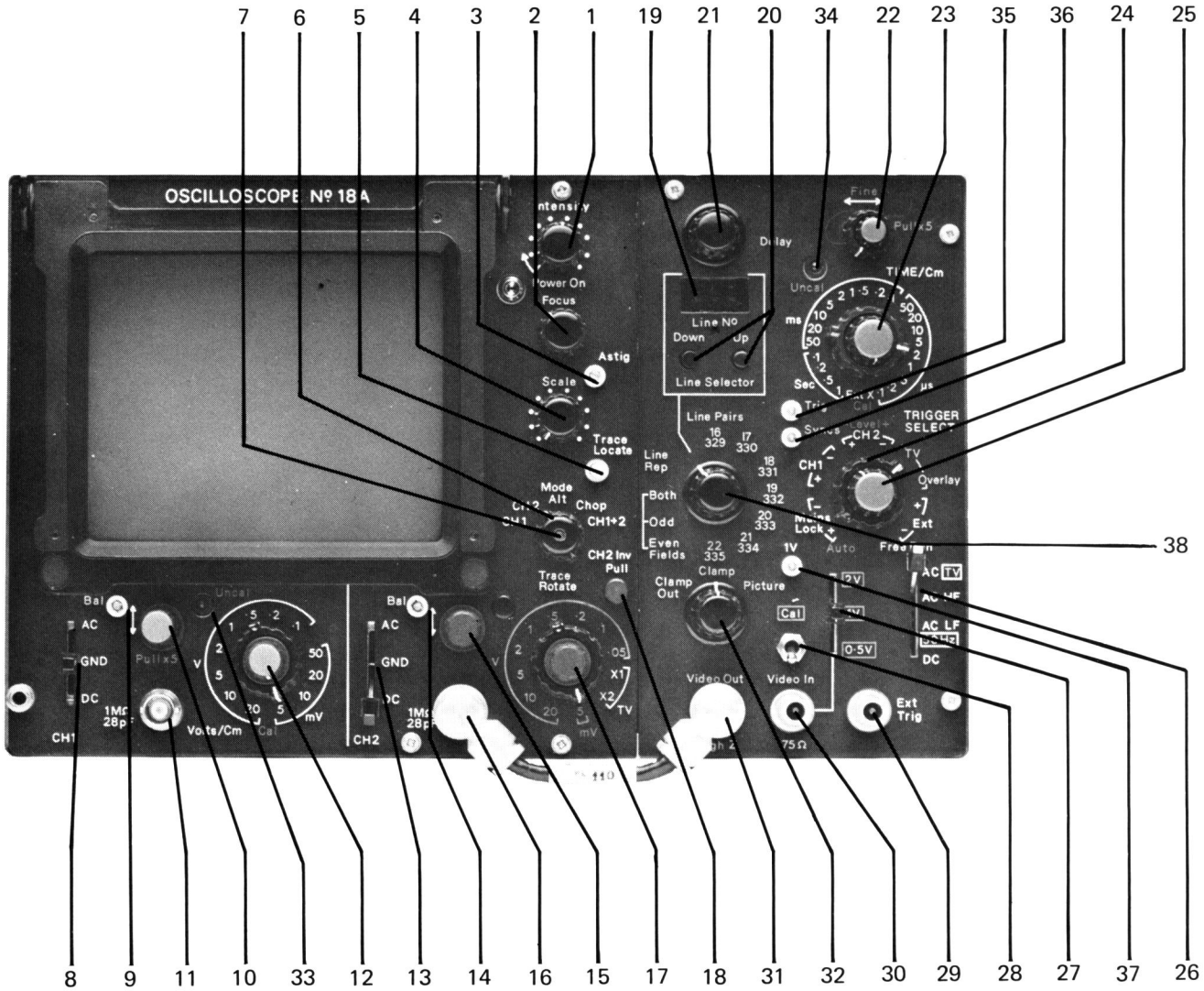
(26) ACTV, ACHF, ACLF 50Hz, DC: A four position lever switch connecting different trigger coupling networks into circuit. ACTV to be used for all TV triggering, except for 50Hz line repetitive test waveforms, when ACLF 50Hz should be used.

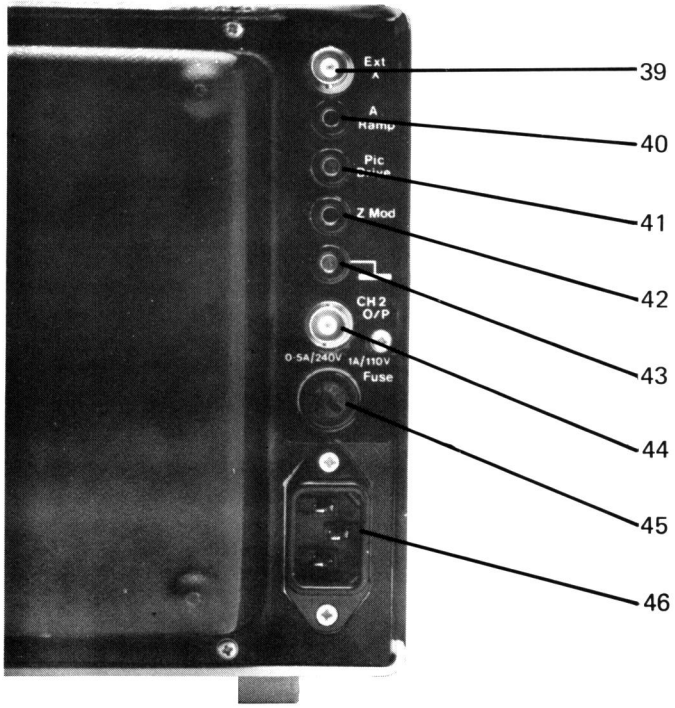
(27) A three-position lever switch providing attenuation of the Video Input signal.

(28) CAL Two position toggle switch permitting either TV input signal display or calibration waveform display on CH2.


7 6 5 4 3 2 1 19 21 20 34 22 23 35 36 24 25
OSCILLOSCOPE Nº 18A
Intensity
Power On
Focus
Astig
Scale
Trace Locate
Mode
Alt
Chop
CH1+2
CH2 Inv
Pull
Trace Rotate
Delay
Fine
Pull x5
Uncal
TIME/Cm
Line Nº
Down
Up
Line Selector
Line Pairs
16 329
17 330
18 331
19 332
20 333
21 334
22 335
Line Rep
Both
Odd
Even Fields
Clamp
Clamp Out
Picture
Cal
Video Out
Video In
75Ω
TRIGGER SELECT
CH1
CH2
TV
Overlay
Ext
Auto
Lock
1V
2V
5V
0·5V
AC TV
AC HF
AC LF
DC
Ext Trig
Bal
AC
GND
DC
1MΩ 28pF
Pull x5
Volts/Cm
Cal
mV
X1
X2
38
8 9 11 10 33 12 13 14 16 15 17 18 31 32 30 29 28 27 37 26


Ext A
A Ramp
Pic
Z Mod
CH2 O/P
0·5A/240V
1A/110V
Fuse
39
40
41
42
43
44
45
46


7 6 5 4 3 2 1 19 21 20 34 22 23 35 36 24 25
OSCILLOSCOPE Nº 18A
Intensity
Power On
Focus
Astig
Scale
Trace Locate
Mode
Alt
Chop
CH1+2
CH2 Inv
Pull
Trace Rotate
Delay
Fine
Pull x5
Uncal
TIME/Cm
Line Nº
Down
Up
Line Selector
Line Pairs
16 329
17 330
18 331
19 332
20 333
21 334
22 335
Line Rep
Both
Odd
Even Fields
Clamp
Clamp Out
Picture
Cal
Video Out
Video In
75Ω
TRIGGER SELECT
CH1
CH2
TV
Overlay
Ext
Auto
Lock
1V
2V
5V
0·5V
AC TV
AC HF
AC LF
DC
Ext Trig
Bal
AC
GND
DC
1MΩ 28pF
Pull x5
Volts/Cm
Cal
mV
X1
X2
38
8 9 11 10 33 12 13 14 16 15 17 18 31 32 30 29 28 27 37 26


Ext A
A Ramp
Pic
Z Mod
CH2 O/P
0·5A/240V
1A/110V
Fuse
39
40
41
42
43
44
45
46

(29) EXT TRIGGER: External trigger source input socket.

(30) VIDEO IN: Input socket for video waveforms. Input impedance 75Ω.

(31) VIDEO OUT: High impedance output socket for linking video waveforms to Channel 2 input.

(32) A three position switch permitting:

a) Display of input TV waveform.

b) As a) but input waveform 'clamped' at black level.

c) TV picture display of input signal.

(33) UNCAL: LED indicating when Channel 1 fine gain control is not in CAL position.

(34) UNCAL: LED indicating when fine control on timebase is not in CAL position.

(35) TRIG: Test point providing feed of internal trig. pulse.

(36) SYNCS: Test point providing output of negative going composite sync.

(37) 1V: Test point providing 1 volt peak to peak calibrated square wave output.

(38) DISPLAY SELECTION SWITCH

(a) Combination of odd and even fields.
(b) Line pairs frame blanking.
(c) Single line selection
(d) Line repetitive.

REAR PANEL

(39) EXT X: Input socket for applying external signal to internal X amplifier.

(40) A RAMP: 4mm socket providing normal timebase range output 0 to +10V from < 10K.

(41) PIC DRIVE: 4 mm socket providing video information for modulating the c.r.t. – linked to Z mod socket.

(42) Z MOD: 4 mm socket enabling a modulating signal to be applied to c.r.t.

(43) ⏚ 4mm earth terminal.

(44) CH2 OUTPUT: Channel 2 output via BNC socket, output 100mV/cm displayed.

(45) SUPPLY FUSE

(46) SUPPLY CONNECTOR

3.2 SWITCHING ON

CAUTION: The Oscilloscope No. 18A is convection cooled and must always be operated in a position such that air circulation through the bottom and top vents is not restricted.

1. For portable instruments set the support/carrying handle to the required operating position. The handle is released by pulling outward both fixing bushes when it can then be turned to lock in any one of 5 positions.

2. ENSURE THAT THE SUPPLY VOLTAGE SELECTOR ON THE REAR PANEL IS SET TO SUIT THE VOLTAGE OF THE SUPPLY TO BE USED:

The selector must not be operated while the instrument is switched on. Connect the supply.
WARNING NOTE: The instrument is designed to operate with its frame earthed and for safety the earth conductor of the supply lead, PL94, must be connected to a safety earth.

3. Turn the INTEN control clockwise beyond the POWER OFF setting and ensure that the indicator lamp lights. A trace should be obtained within 1 minute and full calibrated performance within 30 minutes.

3.3 OBTAINING A TRACE

1. To obtain a trace:

a) Set the MODE switch to CH2.

b) Set the TRIG SELECT switch to FREE RUN.

c) Set the 'VIDEO SEL' to CLAMP or CLAMP OUT.

d) Operate the TRACE LOCATE push button.

e) Centralise the display using the X and CH2 shift controls.

f) Release the TRACE LOCATE button and set the INTEN control for a display of the required intensity.

g) Adjust the FOCUS control and ASTIG preset control to obtain a sharply defined trace.

If the TRACE LOCATE button is operated at any other time, the trace should appear. The appearance of the trace toward the top or bottom of the screen can be corrected by the relevant Y shift control unless there is an excessive Y input signal.

Similarly, deflection to either side in the External X modes can be corrected by the X shift control unless due to an excessive X input signal.

If the timebase is in use, the lack of horizontal deflection suggests incorrect triggering.

Once the trace is centred, the TRACE LOCATE button should be released and any necessary correction made to the INTEN setting.

To minimise the possibility of errors due to spurious trace modulation at the start of trace scan, the trace length overscans the display area by approximately 10%. Before attempting any waveform measurement therefore, it is recommended that the horizontal positioning of the trace be set to finish at the right hand edge of the c.r.t. screen. This is particularly important when measuring the ITS 2T pulse, since spurious modulation is most likely to be a problem at high trace intensities and fast scan rates.

3.4 SETTING UP Y CHANNELS

1. a) Using the VIDEO INPUT with CH2 mode, the

internal calibrator voltage is introduced automatically by setting the calibrator switch to [CAL]. Note that this switch must be reset after the calibration is completed.

b) To calibrate CH1, use is made of the BNC-to Clips lead PL44 to connect the 1V CAL waveform to the CH1 input socket via the "1V" front panel pin.

2. When using either 1a or 1b above, the signal coupling lever switch should be set to DC except where otherwise stated.

3. To locate the baseline, set the lever switch to the GND setting. At this setting, the input signal is open circuit and the input of the amplifier is switched to ground.

4. To adjust the sensitivity on 1a, set the Y gain switch to X1 - - and adjust the variable sensitivity control until the peak-to-peak amplitude of the cal signal coincides with the CAL marks (≡143 divisions) on the vernier graticule. The video input attenuator switch (27) should then be set to the p-p amplitude of the input signal ±0.5V. Thereafter only the variable sensitivity control and X2 switched gain control should be used to increase the display height, otherwise possible overloading of the CH2 input may occur. For CH1 operation, set the "VOLTS/CM" switch to 200mV/cm and adjust the variable sensitivity control until the peak-to-peak amplitude of the 1V calibration square wave occupies 100 division on the vernier graticule.

NOTE: On CH1 and CH2 the range of the VARIABLE control is uncalibrated. A fixed calibrated position is however provided for CH1, a warning UNCAL light mounted adjacent to the VARIABLE control is lit once out of the CALIBRATED position. At the CALIBRATED setting, the calibration corresponds to the setting of the VOLTS/CM switch.

5. For vertical movement of the trace, adjust the Y shift controls (identified with vertical arrows).

6. If, under no signal conditions, trace movement is detected when the VARIABLE is altered, reset the BAL preset control. If there is subsequent movement when the VOLTS/CM control is switched between ranges, the STEP BAL preset control should be adjusted. Access to this control is through the bottom cover.

7. The bottom cover preset gain adjustments for CH1 and CH2 are factory aligned and must not be adjusted by the operator.

3.5 SINGLE TRACE OPERATION

1. For single trace operation on the CH1 channel mode, set:
   a) The MODE switch to CH1.
   b) The CH1 shift control (indicated by double ended vertical arrow) to mid setting.

2. For single trace operation on the CH2 channel mode, set:
   a) The MODE switch to CH2.
   b) The CH2 shift control (indicated by double ended vertical arrow) to mid setting

3. High sensitivity operation with an approximate bandwidth of d.c. to 10MHz can be obtained on CH1 by pulling the SHIFT control which increases the sensitivity 5 times, i.e.

1mV/cm with the sensitivity set to 5mV/cm

2mV/cm with the sensitivity set to 10mV/cm

4mV/cm with the sensitivity set to 20mV/cm

Beyond this it is better to revert to normal operation.

4. When using the VIDEO INPUT facility see Sections 3.4 and 3.9 for the correct operation of the 3-way input attenuator switch in association with the variable and switched Y gain controls on CH2.

3.6 DUAL TRACE OPERATION

In the dual trace condition, the beam switching function is in operation and results in the independent display of two signals simultaneously. Two modes of beam switching – chopped or alternate – are used, selected by the setting of the MODE switch. At any fast setting from 0.1μs/cm to 0.5ms/cm inclusive, the alternate mode is recommended. At slow settings from 1ms/cm to 1s/cm, inclusive, and EXT X, the chopped mode is preferable. For EXT X the chopped mode is essential to give two trace operation.

1. For dual trace operation, set
   a) The CH1 shift control to mid position.
   b) The CH2 shift control to mid position.
   c) Select ALT or CHOP on MODE switch.

3.7 TIMEBASE OPERATION

The speed of the timebase is determined by the setting of the TIME/CM switch. In addition to selection of the speed of the internal timebase, the switch has a functional setting, EXT X in which the internal timebase is inoperative. The gain of the internal X amplifier may be increased by 5 times by pulling out the PULL X5 control on the inner shift control. This facility is available at all settings including EXT X. The facility effectively increases the sweep length from 10cm to 50cm and thus allows close examination of any portion of the trace. Any portion of the increased sweep length may be selected for viewing on the display by adjusting the X shift controls (identified by horizontal arrows). The fine shift control will move the display by approximately 1cm when the PULL X5 is not operative and by 5cm in the magnified mode.

A particular advantage of this facility is to increase the maximum sweep speed to 20ns/cm.

1. To adjust the timescale of the horizontal axis

   a) Set the TIME/CM switch to the required setting.

   b) If necessary, adjust the concentric VARIABLE.

NOTE: The range of the VARIABLE control is approximately 3:1. The VARIABLE control is uncalibrated and a warning light, adjacent to the VARIABLE control, lights in the UNCAL position. At the CALIBRATED setting only, the calibration corresponds to the setting of the TIME/CM switch.

Selection of the 1sec/cm range and full use of the variable control, provides a total sweep time of approximately 0.5 min.

3.8 TRIGGER

The timebase may be operated in a FREE RUN condition or more normally, triggered from the positive or negative slope of a signal as determined by the setting of the TRIGGER SELECT switch. The triggering sources selected by the TRIG SELECT switch are as follows:-

a) The mains power line frequency derived from the internal mains supply transformer, at either + or - slope.

b) CH1± or CH2± amplifiers (irrespective of which beam is displayed), at either + or - slope.

c) T.V. and Overlay. This uses internally generated signals from the VIDEO input.

d) Any external triggering source connected to the EXT TRIG socket.

e) FREE RUN. In this mode the timebase runs continuously but is not triggered.

The level control concentric with the TRIG SELECT switch allows selection of the triggering point on the trigger waveform and hence determination of the start of the horizontal trace. When the LEVEL control is set to AUTO, the trigger circuit automatically biases itself to a sensitive trigger level condition. In the absence of a trigger signal in this mode, the timebase will free run and maintain a displayed sweep at the selected speed. The TRIG SELECT switch is used in conjunction with the TRIGGER COUPLING lever switch. This switch connects different networks into the trigger amplifier circuit and is effective on all settings of the TRIG SELECT switch.

The operating facilities available at the 4-settings of the lever switch are as follows:-

1. AC.TV. This introduces a wideband A/C coupling circuit which should be used when displaying all T.V. signals except line repetitive 50Hz test waveform when AC LF 50Hz should be used and TRIG SELECT switched to CH2

2. AC H.F. A filter is switched into circuit to reject low frequencies. High frequency triggering may be effected from low level waveforms with suitably high ripple content.

3, AC LF 50Hz. A filter is switched into circuit to reject high frequencies and so ensure low frequency triggering, e.g. 50Hz test waveform.

4. DC. A wideband trigger mode, which is most useful at very low frequencies. The Y-input coupling must also be DC for this mode to be effective on internal trigger.

N.B. When EXT TRIG position of the TRIGGER SELECT switch is used there is no T.V. sync separator in circuit, irrespective of the TRIGGER COUPLING selected; note also that neither the OVERLAY nor waveform delay facility is available either.

To operate the instrument in its CH1 mode triggering is effected as follows:-

1. Set the TRIG SELECT switch to the required trigger signal (i.e. MAINS LOCK, CH1, CH2 or EXT).

2. Set the DISPLAY switch to either 'CLAMPED' or 'UNCLAMPED'.

3. Set the TRIGGER COUPLING switch to the required setting.

4. On most waveforms it is convenient to select AUTO. If this is not required, adjust the LEVEL control so that the trace starts at the required point on the waveform. If the timebase is not required to be triggered, set the TRIG SELECT switch to FREE RUN.

NOTE: If, in the Auto mode, the frequency of the trigger is less than approximately 40Hz, or the amplitude is too low for reliable triggering, the timebase automatically changes to a free run condition. This condition produces a trace at the selected sweep speed.

3.9 TV TRIGGERING

The timebase is designed to trigger from positive-going video (negative sync) of 1V±0.5 peak-to-peak amplitude via the VIDEO 1/P socket.

Signal input levels in the range 0.125 volts – 6 volts peak-to-peak may be accommodated by the use of the input attenuator switch (27).

The [1V] position should be used for input signal levels in the range 0.7 volts – 1.5 volts peak-to-peak. Outside this range the [0.5V] and [2V] positions should be used as appropriate.

Waveform Response:

Sin^{-2} Pulse and Bar:-

25μs Bar $\leq$ 0.5%k

2T Pulse $\leq$ 0.25%k

T Pulse overshoot $\leq$ 0.5%

LF Response (50Hz square wave) $\leq$ 0.25%k

Clamped Response:

As above but relaxed by a factor of two. All waveform performance figures confirmed at X2 gain (i.e. 100mm picture height).

The timebase allows the input video signal to be displayed either as a TV picture or as a waveform, clamped or unclamped.

For waveform display, the timebase functions in the normal manner but receives its triggering information from an internal sync separator system.

For the PICTURE requirement the timebase is switched out automatically, and line and field timebases are introduced to generate the required raster.

3.10 OPERATION IN THE 'CLAMP' OR 'CLAMP OUT' MODES

Video waveforms connected to the VIDEO INPUT socket may be examined either in 'clamped' or 'unclamped'

In the CLAMP mode, the video information is locked to Black Level for 0V d.c. on the Y display. Because of the action of the clamp, changing picture content does not affect the position of the mean d.c. level on the Y-display. This makes this mode particularly suitable for viewing waveforms where substantial picture level changes or LF ripple may exist.

Setting up for these functions is accomplished by the following procedure.

1. Check that connecting lead (PL110) is in position between the sockets VIDEO OUTPUT and YCH2. Set mode switch to CH2.

2. Switch to 'CLAMP' or 'CLAMP OUT' mode as required.

3. Set the Y CH2 input to GROUND and the Y gain control to X1.

4. Set the TRIGGER SELECT switch to FREE RUN and centre the Y CH2 trace using the multiturn Y-shift control. Return Y CH2 input select to DC.

5. Set the video input attenuator lever switch to the input signal amplitude and insert the video signal.

6. Set the TRIG SELECT switch as required.

7. Set the TRIGGER COUPLING switch to AC TV.

8. It is preferable to begin by setting the timebase range switch to 10μs/cm so that the display will show about 1½ lines of information.

9. Select the required line or field to be viewed, using the LINE SELECT switch (see section 3.12).

10. Now adjust the trigger level control until a stable trigger on the required line is obtained. This position is approximately central on the control. (The trigger level allows about 90° of angular rotation over which the control may be set for this requirement.)

3.11 DELAY CONTROL

This control becomes effective when TV is selected on the TRIGGER SELECT switch. Approximately 80μs of delay from the trigger point is available.

NOTE: If the DELAY control is not operative when TV is selected, it may be necessary to readjust the Trigger Level control.

3.12 LINE SELECTION

The operator may view if required 7 pre-selected video lines, superimposed as pairs in the range 16/329 to 22/335, by direct access on the switch. In addition, Fields 1 and 2 or both Fields superimposed may be observed. On these selected positions, the first broad pulse of field information is not displayed; and therefore if it is required to observe this, or the equalising pulses preceding it, it will be necessary to use the LINE SELECTOR in conjunction with the l.e.d. display.
LINE REPETITIVE triggering is provided where pulse and bar generators etc. are to be used. In this mode, the sync waveform does not need to contain field pulse information. Triggering is performed on every alternate line. The DELAY control may be used here for analysis of relative pulse heights etc. using the vernier graticule markings.

On the LINE SELECTOR position, an l.e.d. display will illuminate showing the line number on which the timebase is triggering. This may be set to any integer between 1 and 625. The selected number may be increased by pressing the UP button; whereupon the display will step up slowly for the first four digits and then speed up. The DOWN button decrements the line count and functions in a similar manner.

3.13 TV LINE OVERLAY

This facility is intended for use with the line repetitive input signals and is effected by switching the trigger select switch (24) to overlay. At the appropriate timebase speed it will be possible to display a single TV line fixed on screen, with the next adjacent line superimposed and under the command of the 'Delay' control (21). If greater detail is required, it is advisable to use the timex 5X expansion (22) rather than further increase the timebase speed, as trigger delay facility is only available on the superimposed waveform.

3.14 PICTURE DISPLAY

A visual display of the 625 line raster is available when the display switch is set to 'PICTURE'. The raster occupies an area approximately 6.5 x 8cm on the screen.

NOTE: That the full signal content is displayed and with the standard video patterns the first vertical ½cm displays test signals and Teletext information prior to the start of the picture.

The video information for modulating the c.r.t is supplied from the 'PICTURE DRIVE' socket on the rear of the instrument, and is linked to the Z mod socket. The PICTURE DRIVE information contains

all the blanking pulses required during flyback, but a short field blanking period is used to enable the operator to observe Test signals etc. preceding the picture content.

An additional bright-up is applied to the picture which starts approximately 1cm from the end of the previous line and extends along the selected line for the period defined by the DELAY control and is used as a pointer to the selected line or lines. The end of the "pointer" indicates the setting of the DELAY control. On FIELD trigger, this pointer over-rides the flyback blanking. If this feature is not required when viewing a picture, the DELAY should be set to minimum.

The 'PICTURE' mode may be displayed by the following procedure:-

1. Check that coax link PL110 is in position between video out and CH2 input, sockets.
2. Set the Y gain control to X1 and the input to DC.
3. Connect the link (PL106) between the PICTURE DRIVE and Z mod sockets on the rear panel.
4. Set the VIDEO ATTENUATOR lever switch to the desired video input level and insert the video signal.
5. Set the DISPLAY switch to 'PICTURE', adjust the Y shift for a central raster and the Intensity control for the best display.

NOTE: It is not necessary to trigger the timebase for this display mode, however, it is useful to have the instrument set up as in Section 3.10 in order that picture waveforms can be analysed immediately on switching away from the PICTURE position. The 5 x expansion is still available for PICTURE display.

3.15 EXTERNAL X

In this condition, the external signal is applied directly to the Internal X amplifier to produce a calibrated (1V/cm) horizontal deflection via the EXT X socket at the rear of the instrument. Dual trace Y operation is only available if chop is selected. The bandwidth is 2MHz.

1. Set the 'TIME/CM' switch to EXT X.
2. Set the display switch to 'CLAMP' or 'CLAMP OUT'.
3. Connect the signal to the EXT X socket.

3.17 CALIBRATION WAVEFORMS

CAL 1V OUTPUT AND INTERNAL CAL WAVEFORM

The 1V output pin provides a d.c. coupled +ve going square wave signal of 1V ±1% at 1kHz. The source impedance is 1kΩ and the signal rise time 100ns approx.

The signal can be applied, via a suitable connecting lead, to CH1 input for Y amp sensitivity set up (see also para 3.4).

VIDEO INPUT mode: When the VIDEO INPUT mode is used, calibration is carried out by operating the CAL switch to [CAL] . This automatically applies 250mV ±0.5% of the 1kHz square wave to CH2 input (and disconnects the 75Ω VIDEO INPUT circuit) also switching the timebase circuits to a free-run mode. (The 250mV cal voltage is 12dB w,r,t, 1V and is set at this level to allow for the 12dB attenuation which is present in the circuitry between the VIDEO INPUT and the VIDEO OUTPUT sockets whether the clamp is in operation or not, *when the VIDEO ATTENUATOR is set to 1V.* This procedure is therefore equivalent to having 1V present at the VIDEO INPUT socket. The 250mV must be so applied to CH2 input since this is high impedance and not directly to the VIDEO INPUT since this is at 75Ω. The 12dB of attenuation not calibrated by this procedure has a negligible uncertainty tolerance.

The visual presentation of the square wave with a free running timebase is a pair of parallel horizontal lines.

The exact settings for calibration of the VOLTS/CM controls are detailed in para. 3.4.

In short, the peak-to-peak amplitude of the calibration waveform c.r.t. display corresponds to the voltage range selected on the video input attenuator. e.g. If [2V] is selected on the video input attenuator then the peak-to-peak amplitude of the calibration waveform c.r.t. display 2V signal input corresponds to 'VIDEO IN'.

3.18 ADDITIONAL FACILITIES

Z MOD

This socket on the rear panel in addition to providing a link for the picture modulation also allows d.c. coupled signals to be applied to the tube.

The c.r.t. trace is intensified by a negative input, and blanked by a positive input. The required amplitudes are:-

a) 2 volts for visible intensity modulation.

b) +20 volts for blanking at normal intensity.

This facility is available in any operating mode of the instrument except PICTURE.

RAMP

This socket on the rear panel provides a d.c. coupled positive-going timing ramp or approximately 10V amplitude, generated by the timebase. The source impedance is 4.7kΩ and the ramp may be used for instance as a drive for external frequency swept oscillators to allow a display of voltage against frequency.

3.19 WAVEFORM MEASUREMENT TECHNIQUES

When using the Oscilloscope No. 18A to measure small amounts of distortion on test waveforms such as the sine squared pulse and bar signals, a useful measurement technique is to use the second input channel, CH1, to provide a reference line or pair of lines on the c.r.t. screen and so

help avoid parallax errors. The following description is a method of using this technique to measure droop on a bar top. Pulse overshoot etc. can also be measured using this technique.

With the video signal applied to the video input and the timebase triggered as necessary to view the full width of the bar top, select dual channel operation as ALT (or at low repetition rates CHOP). If the CH1 input coupling is set to GND, a single horizontal line is superimposed on the bar. Adjust the CH1 shift control to position this reference trace on the left hand end on highest point of the bar top to be measured. It is now easy to detect on the bar top small variations from the reference line and to measure the deviation against the graticule.

An extension of this technique provides two reference lines for more accurate assessments of small deviations.

Connect the CH1 input directly or via a probe to the CAL output pin of the Oscilloscope No. 18A. If a probe is used first check that it is correctly compensated. Set the CH1 input coupling to d.c. As this calibration signal is not synchronised to the video input signal used for trigger, its square wave shape will appear as two parallel lines. Operate the CH1 VOLTS/CM, VARIABLE sensitivity and shift control to position these two lines to correspond to the maximum and minimum points of the bar top under observation. Without altering the position of the VARIABLE control, increase the CH1 sensitivity by 3 switch positions to increase the spacing of the reference lines by 10 times. Operate the CH1 shift control to align one of the lines with a graticule line and measure their spacing against the graticule. The peak-to-peak waveform aberration (the original spacing of the reference lines) is then one tenth of the final measured spacing which can be expressed as a percentage amplitude of the original waveform.

It should be realised that actual voltage measurements of pk to pk aberration are calculated with respect to the CH2 sensitivity and the actual setting of CH1 sensitivity is irrelevant to the measurement.

To improve discrimination of waveform aberration measurements, it is possible to overscan the 8cm vertical scale to 150mm without introducing distortion to a conventional sine squared pulse and bar.

A further variation to this technique of using the second channel as a reference is to drive it from any other square wave source diplexed with a calibrated d.c. source. The aberrations in a vertical direction can thus be measured in terms of d.c. calibrated shift.

Circuit Description

Section 4

4.1 THE BLOCK DIAGRAM

The block diagram for the complete instrument is shown in Fig. 1. It is not intended to be a full logic diagram but details the functional points of the circuit and their interrelation. The circuit can readily be divided into two main sections which are the Y and the X deflection circuits. The latter includes the timebase with the associated trigger system and the video signal and synch separator system. The bright-up or Z modulation function is described as part of the timebase function.

The main X and Y signal paths for a dual trace display using the main time sweep only, are indicated by the heavy lines.

Y CHANNELS

The switch attenuator, pre-amplifier and trigger amplifiers are identical for the two Y channels. CH1 differs in having invert and output facilities. The state of the decade steps of attenuation and 1, 2, 5 sequence of pre-amp gain switching are determined by the sensitivity selected.

The use of the x5 GAIN of CH1 increases its basic sensitivity to 1mV per centimetre.

The channel switch is a fast electronic switch with the equivalent of a change-over action as shown. It selects either the CH1 or the CH2 signal to be passed to the subsequent stages and is controlled from a bistable. In the chop mode the bistable is driven by continuous pulses from the free running multivibrator, switching the beam between the CH1 and CH2 signals as the X sweep progresses. In the alternate mode, the multivibrator acts as a monostable generating a single pulse to reverse the beam switch at the end of each timebase sweep, giving alternate CH1 and CH2 sweeps. In the ADD mode, both the CH1 and CH2 switches are closed and the two signals are summed algebraically. On CH1 and CH2 only the appropriate switch is closed allowing that signal to pass.

The signal from the selected channel is passed via amplifiers to the Y deflection plates of the c.r.t.

THE EXTERNAL X I/P

When external X is selected, the trace is brightened and the timebases are inhibited. The amplified X input signal passes through the X gate to the main amplifier.

THE TIMEBASE

The purpose of the timebase system is to generate a linear ramp to deflect the spot in the X direction. The trigger system initiates each sweep from the incoming or other signals, normally to obtain a stationary display of a repeated waveform.

The internal or external signal as selected is amplified by the trigger amplifier to drive a trigger circuit. If the timebase is ready to commence a sweep, a transistion of the trigger circuit will set the timebase bistable which in turn initiates the ramp. The signal is passed through the X gate and X output amplifier to the X deflection plates of the c.r.t. At the end of the sweep, when the ramp reaches the required level the bistable is reset, returning the ramp to its original level. During the period of sweep the trigger gate is prevented from passing trigger pulses to the bistable and this inhibition is maintained by the hold-off circuit until the ramp generator is fully recovered, ready for the next sweep to commence on the next trigger pulse, when the cycle repeats.

The bright-up amplifier normally holds the c.r.t beam in the cut-off state. The output of the bistable which allows the ramp to operate, also feeds the bright-up amplifier to raise the intensity of the c.r.t. spot to the level determined by the intensity control.

At the end of sweep this output of the bistable is reset and blanks the trace during the flyback period. If the Y channels are being switched in the chopped mode, the differentiated output of this multivibrator is also fed to the bright-up amplifier to blank the trace while the Y switching transition takes place. This leaves the appearance of two separate traces for CH1 and CH2 on the screen unless the sweep speed is higher than that normally required for chop operation.

TIMEBASE TRIGGER MODES

The trigger signal for the timebase selected from internal, external, TV or mains power supply frequency sources, is a.c. or d.c. coupled before being fed into the trigger amplifier. This is biased by the required trigger level and the resultant output passed to the trigger circuit where the waveform is squared up.

In the FREE RUN mode the trigger gate is permanently energised, and the timebase bistable is set again at the end of each hold-off period.

When AUTO coupling is selected, the trigger amplifier is automatically biased to the optimum working point for sensitive operation of the trigger. If the signal level out of the trigger amplifier is insufficient to operate the trigger circuit, a further output from the auto circuit causes the timebase to free run, displaying the necessary bright line trace.

TV OPERATION

In all TV modes of operation, the oscilloscope is driven from the signal applied to the VIDEO INPUT socket. The signal is fed to a three position 75Ω attenuator. In the CLAMP-OUT mode, the output from this attenuator is switched directly to the VIDEO OUTPUT socket which is coupled externally to the CH2 input socket for display against the timebase.

The output from the attenuator is fed also through a buffer amplifier to a black level clamp amplifier and the output from this is selected as the VIDEO OUTPUT when the Display Select switch is set to the CLAMP mode. The level clamped signal also drives a comprehensive sync separator system which is described in detail later. When the PICTURE mode is selected the VIDEO OUTPUT signal is derived from the Field Ramp Generator.

To complete the necessary raster, the sync separator circuit drives a Line Ramp Generator. The output of this is switched into the X deflection amplifier in place of the normal timebase sweep signal by the X Gate. The clamped video signal, buffered through video drive amplifier has to be linked externally from the PIC. DRIVE to the adjacent EXT Z MOD input to complete the picture display.

DELAY/OVERLAY

When either of the TV modes is selected by the Trigger Source switch, the timebase is triggered from the sync separator system via a delay monostable. In the TV position the output from the monostable is taken via an inverter to the Timebase Trigger introducing a delay as determined by the monostable period and set by the delay control. This has a single range of approximately 80μs.

In the OVERLAY position both the Delay Edge and the Undelayed edges from the Delay Monostable are alternately gated via the inverter to the Timebase Trigger. The result of this is that alternate sweeps are overlaid; with the delay facility retained on one sweep test signals consisting of pulse and bar components may be evaluated.

In the PICTURE mode, an additional bright-up signal is applied to the Z modulating signal during the delay period and this is used to identify a line or lines selected by the TV trigger system. The length of this bright-up line indicates the delay period pointing to that section of the video waveform which will be displayed against the timebase on switching from PICTURE to the CLAMP or CLAMP-OUT modes of display.

SYNC SEPARATION

A portion of the video signal is taken off the video attenuator output and amplified by about 5 times. The high frequency components of this signal (above 4.4MHz) are removed by a low pass filter, i.e. the Chroma and sound signals. The filtered signal then passes to the line sync separator. This stage consists of two circuits; a primary sync separator which sets up the initial conditions, and a secondary sync separator in a regenerative loop with a clamp monostable multivibrator to provide a hard lock.

The primary sync separator provides sync pulses to operate an internal black level clamp operating during the back porch period of the video waveform, so d.c. restoring the signal. The secondary sync separator receives the clamped video and feeds sync pulses to a 50μs monostable multivibrator. Since this circuit has a time period exceeding the half-line periods (32μs) during the Field sync period, only the full line sync pulses at 64μs intervals are allowed to pass through it. The undelayed leading edge from the monostable (coincident with the leading edge of the line sync pulse) is fed to the clamp monostable. This has a period of 5μs and provides a delay just exceeding the line sync pulse period (4.8μs). A second clamp operating during the back porch period is actuated by the delayed edges from the output pulses of this monostable, thus providing the regenerative lock action with the secondary sync separator.

Field sync separation from Composite Sync information is achieved by a single transistor amplifier with RC coupling at both its input and output. The time constant of the input circuit to the stage is chosen such that it only responds to the broad Field Sync pulses which cause a change of mean d.c. level. The output RC network operates in such a way as to only select the narrow 4.7μs gap occurring between the first and second broad Field sync pulses.

Even Field (F1) and Odd Field (F2) pulses are separated by gating the detected field pulse with the two outputs from the 50μs monostable. The First Even Field Broad pulse begins in phase with the position normally associated with the leading edges of the line sync pulses, whereas the Odd Field pulses begin half a line period late. Since the gap between the first and second broad pulses occurs 27.3μs after the leading edge of the first Broad pulse, then the Even detected field pulse occurs within the 50μs time period of the monostable.

The Odd field detected pulse, however, occurs 59.3μs after the phase position of the line sync pulses, and therefore outside the time period of the monstable. By comparing inverted and non-inverted outputs from the monostable with the detected field pulse, then F1 and F2 pulses can be discriminated. Outputs from the Line and Field pulse separators are then used to drive the Line and Field ramp generator circuits used for the PICTURE mode.

LINE COUNTER SYSTEM

The 50μs monostable which provides a regular pulse train in phase with the leading edges of line syncs is used to drive the line counter. The delayed edge of the monostable is used to clock the counter; and hence clocking occurs after about ¾ of the line period has occurred. The 625 line counter consists of a 12 bit binary counter which for all modes except when the line selector display is required, is reset by the F1 field sync pulse. When the line selector display is to be used by selecting the appropriate position on the LINE SELECT switch then internal gating is arranged for the counter to make it count to 625 independently of the position of the incoming F1 sync pulses.

LINE SELECT SWITCH POSITIONS

1. EVEN, ODD AND BOTH FIELDS TRIGGERING

These switch positions select either the output from the Field Sync separator or the F1 or F2 outputs from the Field pulse discriminator to be the input for the trigger DELAY monostable.

Since the detected field pulse occurs in the gap between the first and second broad pulses then information prior to this within the field period, (e.g. the first set of equalising pulses) cannot be displayed in these 3 switch

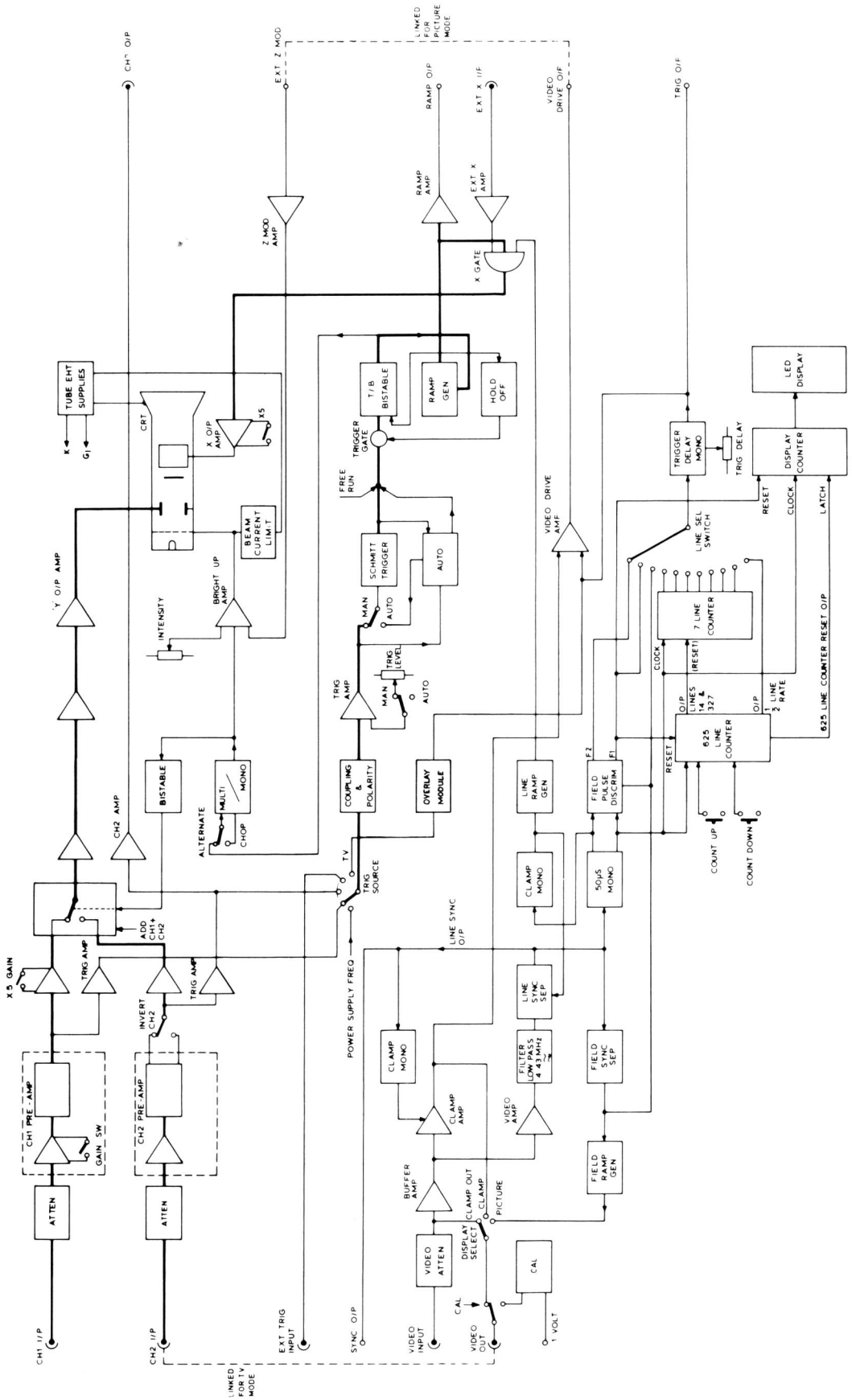


Fig. 1 Block Diagram

positions; and therefore for such requirements the line selector display position should be used.

2. LINE REPETITIVE TRIGGERING

This position is useful for displaying waveforms from Pulse and Bar generators which produce repetitive line-by-line picture information. The first bit (Q1) output for the counter is used to trigger the DELAY monostable on this switch setting. This provides the monostable with triggering on alternate lines, thus preventing an overlap problem when the monostable DELAY period is extended to maximum. Note that the 625 line counter is normally reset by the F1 Field sync pulse, however, some pulse and bar generators do not produce Field information, and the system will operate satisfactorily without such reset.

3. LINE SELECTOR AND DISPLAY

The line selector and display is useful in that any of the 625 lines may be individually selected, with a numerical counter displaying the number of the selected line.

In this mode the 625 line counter provides its own reset signal when the 625 count is complete and then commences counting again. The position of the reset pulse with respect to that of the F1 sync pulse is random, although constant as long as the counter maintains its 625 count. By pressing either of the count UP, or count DOWN push buttons below the l.e.d. display the counter is made to count to either 626 or 624 respectively, for a short period thus altering the position of the counter reset pulse with respect to the field F1 pulse. A completely independent counter which drives the l.e.d. display is clocked by the same line rate pulses which drive the 625 line counter and latched when the 625 line counter resets. The display counter, which is reset by the F1 field pulse, then counts the number of line rate pulses which have elapsed between the F1 pulse and the 625 line counter reset, and indicates the count on the l.e.d. display. In order that trigger is provided prior to the selected line on the display the 624th count is gated out to the DELAY monostable. Since the counters are clocked 50μs after the leading edge of line syncs, timebase trigger will occur about 10μs before the next line pulse appears, thus enabling the operator to view a complete line of picture information.

4. SELECTED LINE PAIRS – 16/329, 17/330 up to 22/335

A superimposed line pair from 16/329 etc. up to 22/335 may be viewed by using the 7 appropriate positions of the LINE SELECT switch. These lines are generally of interest for viewing Teletext data and test signals which precede the main picture information. It is convenient to use the LINE SELECT switch for viewing these lines, instead of using the line selector display since instant access is available. The seven tapped outputs for these line pairs arrive at the DELAY trigger monstable from a ten stage Johnson type counter via the LINE SELECT switch. The counter has a feedback arranged on it so that it actually counts to 9 and then stops. It must be then reset before it can commence counting again. In common with the 625 line counter and the Display counter it is clocked by the delayed edge from the 50μs monostable multivibrator. It derives its reset from gated outputs from the 625 line counter which occur on counts of 14 and 327. The reset is held high until either of these counts has occurred. When the reset has dropped low the counter then commences clocking on line 15 or 328. Since the counter is clocked about 50μs after the start of the 15 or 328th line the Q1 output rises high about 10μs or so before the 16th or 329th line. Similarly, the Q2 output goes high before the 17th/330th line and so on.

The timebase then gets triggered via the DELAY trigger monostable just prior to the start of the selected line pair.

by means of the two networks, R226/R227 and R231/R232.

3. The maximum sensitivity of both CH1 and CH2 channels can be increased to 1mV/cm, this requires that the gain of these stages is increased by five times and is achieved by shunting across the emitter circuit the network, R228/R229, for CH1 and R233/R234 for CH2. The switch for this function is mounted on the rear of the respective shift controls.
4. Networks, R230/C202 and R235/C206, are included to allow the h.f. response of the two channels to be matched.

The signals from this pair of amplifiers are fed to the beam switch circuit consisting of eight diodes, D201 to D208, inclusive. The switch is operated by signals applied in anti-phase to points 26 and 29 from the Beam Switch bistable. The signal level at these points switches from approximately +7V to approximately +0.3V. Thus when point 26 rises to +7V diodes, D201 and D202, are cut-off and diodes, D203 and D204, are turned on, allowing CH2 signals to pass to the following stage. At the same time, point 29 will be at approximately +0.3V, allowing D205 and D206 to conduct and prevent CH2 signals reaching the following stage. When the potentials on points 26 and 29 reverse, CH2 signals will pass to the following stage and CH1 signals will be blocked.

The output from the beam switch network is taken to transistors, TR210 and TR211, connected as shunt feedback amplifiers with R249 and R250 providing feedback from the collector to base of the respective transistor. Provision is also made in this stage by means of A.O.T. resistors, R294/R295, to take out small unbalances which cause excessive trace movement when switched to the ADD mode. Also in the ADD mode it is necessary, since two stages are now connected to a common load, to remove half the resultant current in the load, this is achieved by returning R245 and R246 to the −15V line when switching to ADD.

Signals from this stage pass to the delay line driver, a further long-tailed pair, TR212/TR213, fed from a constant current source, TR214. A current of 10mA per side is common to this stage and, via the delay line, to the delay line terminating stage.

The Beam Switch bistable consists of transistors, TR215 and TR216, the conducting stage of these determining which channel is displayed. For single trace operation, either of the emitters is grounded via points 35 and 36. For dual trace operation, both emitters are grounded and the transistors are turned on or off by pulses from TR217 routed via capacitors, C213 and C218, and diodes, D212 and D211. In the ADD mode both emitters are open circuited raising both collector voltages and hence opening both diode gates.

The chop multivibrator contains transistors, TR217 and TR218, which operate as an emitter-coupled astable multivibrator, whose frequency of approximately 500kHz is determined by R280, R285 and C221.

In addition to operation for the chop function, the circuit acts as a monostable when the alternate mode of beam switching is selected. In the alternate mode, the circuit produces 1 pulse per timebase sweep and is fed with an end-of-sweep pulse from the timebase bistable. The −15V volts supply is connected to point 32 via the FUNCTION SWITCH, this increases the current through TR218 and causes a drop in the level of the collector voltage.

This drop cuts off TR217. The negative-going end-of-sweep pulse thus finds the circuit in a monostable condition which it triggers, producing a high amplitude positive-going pulse at the collector of TR218 and a negative-going pulse at TR217. The output from TR218 is taken to the Bright-up Amplifier to blank the trace during the chop transition period and that from TR217 to the Beam Switch bistable.

4.4 DELAY LINE AND DELAY LINE EQUALISER

The Delay Line is of the wound type and introduces a signal delay of approximately 95ns. This time allows for delay in the timebase and bright-up circuits and ensures that the first part of a signal is visible.

The output of the delay line is terminated by the resistors, R301 and R302, and feeds into the common base stage, TR300 and TR301.

The Pulse response compensation for the delay line is provided in the following stage, TR302/TR303, by means of resistance/capacitor networks, R308/C302, R309/C303, R310/C305, R311 and C306, connected between the emitters.

A further stage, TR304/TR305, provides additional frequency compensation (C310, C311, R324/C312) and raises the signal to the required level to drive the output stage.

4.5 OUTPUT STAGE

The output from TR304 and TR305 feeds the grounded base pair, TR356 and TR357. From this stage the signal drives into the differential input pair, TR351 and TR352. These two transistors, together with TR353 and TR354, operate a differential cascode amplifier.

The collector loads are made up of two resistors in series in order to give the required dissipation with minimum stray capacitance. High frequency compensation is provided by the inductances, L351 and L352.

A constant current transistor, TR355, gives a current in each side of the output stage of approximately 25mA and holds this stable against small variations of the dc input level of +2.4V. At this current the nominal mean Y plate potential is +75V.

4.6 Y TRIGGER AMPLIFIERS AND CH2 OUTPUT AMPLIFIER

Incorporated on the Beam Switch printed circuit board are the CH1, CH2 and composite, trigger amplifiers and the CH2 output amplifier stage.

The CH1 and CH2 trigger amplifiers consist of long-tail pairs, TR201/TR202 and TR207/TR208, receiving differential signals from the CH1 and CH2 pre-amplifiers and providing single ended output for the timebase.

R213 and R223 provide a means of setting the dc level for the trigger circuits (nominally 0V).

In addition a further output is taken from the CH2 trigger amplifier and fed to an amplifying and inverting stage, TR209. This provides an output level of 100mV/cm and when used in conjunction with the X amplifier, gives an X-Y operation facility.

The gain of this stage can be set by R238 and phase shift correction is provided by C228 connected across the feedback resistor, R242.

4.7 TRIGGER SELECTION AND AMPLIFICATION

Trigger sources (CH1, CH2, TV, LINE, EXT.) are taken to S40AF. The internal trigger signals are brought via 50Ω coax, and are terminated by R400, R406 and R577. TV trigger signals are derived from the Delay Monostable, IC617a, and attenuated by R725 and R577. The Line trigger signal is provided from a single turn secondary winding on the mains transformer and the correct trigger voltage is obtained by the simple attenuator, R405 (mounted on S40), and R773 on the main TV logic board. External trigger signals are attenuated approximately fifty times by the network R401, C400, R402 and C401. The signal selected by S40AF is passed via the trigger coupling switch, S42, to two cascaded emitter-follower stages, TR409 and TR410. D406 and D407 provide the necessary protection against excessively large external trigger signals. The signal from the emitter of TR410 is switched by S40BF and S40BB according to the selected trigger slope, to the base of TR413 or TR414, which form a long-tailed pair amplifier. S40BF, S40BB also connect the undriven base of this amplifier to the network, C451, R437 and R438 which provides a low impedance path to ground for high frequency signals and the correct bias to balance the amplifier. The trigger level control (R440) also acts on this network via R441, introducing a positive or negative offset, which is thus mixed with the amplified trigger signal.

The network, R557, C454 and C415, between the emitter of TR413 and TR414, provides high frequency compensation. The output from TR414 is applied to the base of TR415 which together with TR416 forms another long-tailed amplifier, R488. R490 determines the gain and C424 provides high frequency compensation. The base of TR416 is normally held at a fixed bias by zener diode, D423, except when S41b (the auto level switch) is open (see Auto operation). When the level control (R440) is adjusted so that the base potentials of TR413 and TR414 are equal, R453 adjusts the dc potential on the base of TR415 so that the Schmitt trigger circuit is brought near its switching point, maintaining the same trigger level for positive and negative slope selection.

The output from the collector of TR415 is taken via D402 and R571 (see trigger signal routing) to the grounded-base amplifier, TR404, and from the collector of this transistor via D401 to the Schmitt trigger circuit. The output from TR416 collector is connected to the auto level circuit.

4.8 AUTO

When auto is selected by turning the 'A' trigger level control to its extreme anticlockwise position, S41a and S41b open. R491 and the base of TR416 are disconnected from the zener diode, D423, so that the dc potential set by R453 has little effect on the amplifier, TR415 and TR416. The opening of S41 causes the potential at the extreme anticlockwise end of the level control to change from −15V approx. to 0V approx. (R440 and R552 form a potential divider across the ±15V lines.) Thus the amplifier, TR413/TR414, is still approximately balanced. S41a also operates on TR403 (see Trigger signal routing) to energise the bright-line circuit. (See free run and bright-line circuit.) Trigger signals from the collector of TR416 are coupled via C411 and C412 to the bases of the complementary amplifier stage, TR406 and TR407. Emitter resistors, R426 and R427, define the gain, and C442 and C443 provide high frequency compensation. Both transistors are normally biased off but are sensitive to small input signals with one or the other being turned on. The output resultant from the commoned collectors is an amplified form of the input whcih is not paralysed by inputs of widely differing mark/space ratio. It is applied via D416 to grounded base stage, TR404, and thence to the Schmitt trigger.

4.9 TRIGGER COUPLING

The selected trigger signal is taken to the coupling switch, S42, where a simple filter is connected into the signal path on all modes except dc coupled. In the ac connection, C402 removes the dc component. In the HF reject mode the time constant of R407, C466 rolls off the response of the amplifier to high frequency signals. In the LF reject position the trigger signal is coupled via the small value capacitor, C403, whose impedance at low frequency forms an effective attenuator with the input resistor of the trigger amplifier to LF signals.

4.10 TRIGGER SIGNAL ROUTING

The different trigger circuit connections, manual or auto trigger, are controlled by the state of TR403/TR405, and the position of the trigger coupling switch, S42. In manual operation, S41a is closed and with no voltage across its base resistor, R552, TR405 is cut off. Current through R420 and R421 turns on TR403 causing its collector potential to become approximately 15V. Current through R424 and D410, pulls the collector

potentials of TR406 and TR407 negative, cutting off D416, and disconnecting the auto circuit output from the grounded base amplifier, TR404. Current through R418 acts on the bright-line circuit (see Free run and bright-line circuit), to prevent it operating. Trigger signals from TR415 are passed to the Schmitt trigger as current from TR415 flows through D402 into TR404, and from the collector of TR404 via D401 to the Schmitt trigger.

When Auto is selected S41a is open, base current through R552 bottoms TR405, and this in turn cuts off TR403. Current through R408 and D435 causes the collector of TR415 to go negative, cutting off D402. At the same time, the current through R424 and D410 is removed allowing the collector potentials of TR406 and TR407 to rise, turning on D416. Trigger signals now pass from the collector of TR416 to the auto circuit, TR406 and TR407, and then via TR404 to the Schmitt trigger. Also, when TR403 is cut off, current through R418 is removed, energising the bright-line circuit, TR411 and TR412, and diode, D404, is turned on by current flowing through R422 enabling the Schmitt trigger output waveform to drive C407. (See Free run and bright-line circuit.)

4.11 SCHMITT TRIGGER

This consists of TR401, TR402 and associated components. When the base of TR401 is negative with respect to ground, TR401 is off and TR402 is on.

R471 and R416 bias the base of TR402 about 0.5 volt positive. When the base voltage of TR401 is driven positive it will start to conduct. R416 provides positive feedback causing a rapid transition to the opposite state with TR401 conducting and TR402 cut off. When the base of TR401 returns negative, the switch-over will occur at a lower level because of the change in potential across R416. This backlash prevents the trigger from responding to low level noise when biased to its operating point.

C404, R414 and C405 provide high frequency compensation of the feedback network. The output from the collector of TR401 is taken via D404 and C407 to the bright-line circuit.

Trigger pulses are applied via C420 to the shunt feedback amplifier, TR438, with R470 as the gain defining resistor. C420, R470 form a differentiating network such that pulse edges appearing on the output of the Schmitt trigger result in positive and negative impulses appearing at the collector of TR438, and these are applied via R467, C423, D420, to one input of the timebase bistable. TR437, connected between base and emitter of TR438 is activated by the hold-off circuit (see section 4.14 HOLD-OFF).

BRIGHT-LINE AND FREE RUN

The bright-line circuit detects the absence of Schmitt trigger pulses and applies a dc trigger to the ramp bistable. It operates only when the AUTO function is selected. S41a opens, turning TR405 on, which applies a small forward current to D404. If no trigger pulses are present the emitter of TR412 is at approximately −3V, holding TR417 off, allowing current to flow via R574, R472, to the input of the shunt feedback stage, TR438, driving its output low, acting as a dc trigger on the ramp bistable. A negative transition of the collector of TR402 is transferred by D404, C407 and D415 to the base of TR411. As this transistor turns on, the rise of its collector potential is transferred via TR412, D418 and C418, in a regenerative loop to its emitter, so that TR411 bottoms, and the emitter of TR412 follows. The regenerative action then ceases and TR411 is turned off, but its collector potential falls slowly as C418 is discharged by R430. TR412 again acts as an emitter follower. However, the regenerative action caused by any trigger pulse can be initiated at any point in the discharge of C418, and when the timebase is being triggered at medium and high frequencies, the system is permanently biased in the condition which allows normal triggered operation.

4.12 TIMEBASE BISTABLE

TR419 and TR420 form the emitter-coupled trigger bistable. R470 normally biases on TR419 and the low potential across R479 holds off TR420.

A negative transition from the Schmitt trigger is coupled via C420 and D420 to turn on TR419. The positive movement of the collector of TR419 is transferred by R479 to hold on TR420 and the bistable is reversed.

The collectors of TR421 and TR422 provide the two buffered outputs from the bistable. TR421 provides the bright-up current pulse to the bright-up amplifier. The alternate beam switching pulse is provided from TR422 via C432 and emitter-follower, TR430. When TR420 is turned on, its collector potential falls and the diode, D422, conducts to initiate generation of the ramp as described in section 4.13. The effect is that the emitter of TR432 goes negative until D431 is brought into conduction when TR420 is turned off and the bistable reverts to its initial condition, ready for the next trigger pulse via D421.

4.13 RAMP GENERATOR

The basic ramp generator is the bootstrap feedback circuit formed by FET, TR426, as a source-follower with two subsequent emitter-followers, TR427 and TR428. The base-to-emitter voltages of these two transistors are approximately equal and opposite so that the emitter of TR428 follows any change of gate voltage on TR426 with an offset which is the gate to source voltage of TR426, plus the potential across R514. The current in TR426 and hence the voltage between its gate and the base of TR427 is held constant, independent of actual potential as this current is the collector current of the grounded-base transistor, TR435.

Consequently there is a constant voltage across the selected timing resistor, Rt, which in the absence of other influences, flows to ground through the selected timing capacitor, Ct, causing the voltage across this capacitor to drop linearly. This linear ramp appears similarly on the

emitter of TR428, is transferred to the emitter of TR432 and goes via the diode gate, D432 and D433, to the X gate. It is also tapped off via R547 to the ramp output amplifier, as described in section 4.22.2.

The sweep speed, that is the ramp slope, is determined by the values of Ct and Rt which are selected for a particular range. Details of this range switching are shown in Fig. 5.

The third factor to control the sweep speed is the gate-to-source voltage of TR426. This FET is matched in characteristics with TR425. As both devices carry the same current being coupled via the grounded base transistor, TR435, and as R512 is equal to R514, the voltage between the gate of TR426 and the base of TR427 is equal to the voltage between gate and source of TR425, plus the voltage across R512. The latter voltage sum is set by resistor network, R511, R508 and R509, together with the preset calibration control, R510, and the variable sweep speed control, R507. When the variable control is moved from the CALIBRATED position, S74 closes enabling the led, D441, to light.

During the flyback period when the timebase bistable is reset, D422 is biased off and current flows through R540 into the emitter of TR431 and so to D429. This current is much greater than the current through Rt, so that the timing capacitor, Ct, is charged rapidly positive, and the emitter of TR428 follows until it approaches zero potential. At this point, TR429 conducts, diverting current from TR431. This subsequent reduction of the current in D429, limits when it balances the current through Rt. This is the quiescent point of the ramp generator with the emitter of TR428 and the collector of TR435 approximately at zero, and the voltage on the gate of TR426 at +4V. When the timebase bistable is switched by a trigger pulse, D422 is turned on, removing completely emitter current from TR431 and reducing the current in D429 to zero. The normal ramp action then takes place with the constant current through the timing resistor, Rt, negatively charging the capacitor, Ct. The capacitor charges linearly until the emitter of TR432 is at about 4V, when D431 conducts to reset the timebase bistable and complete the cycle.

4.14 HOLD-OFF

Triggering of the timebase bistable must be prevented or held-off during the flyback period until the ramp generator has fully returned to its quiescent state. When a trigger pulse switches the timebase bistable, TR419/TR420, the collector potential of TR419 goes positive and, acting through R448, turns TR437 on, presenting a low impedance path to ground to inhibit trigger pulses through C420. The capacitor, CH0 (representing the next smallest timing capacitor in the timing series Ct) is charged negatively by the negative-going ramp on the emitter of TR432, via gate, TR423/D425/D426. TR423 is only turned on by the timebase bistable during the sweep, via R481, and ensures that CH0 starts to charge immediately the ramp is initiated.

As CH0 charges negative, TR418 is cut off and the current in R466 flows through R458 to cause TR437 to conduct. At the end of sweep when the timebase bistable is reset, TR423 is cut off, removing the charging current from CH0. Current through R468 slowly discharges CH0.

While the sweep generator is in its flyback period, CH0 holds TR418 cut off, leaving TR437 in conduction to inhibit trigger pulses into the timebase bistable. After the ramp generator has reached its quiescent condition, CH0 discharges sufficiently to allow TR418 to conduct and cut off TR437, allowing D420 to conduct on the next trigger pulse to initiate another sweep.

4.15 SYNC SEPARATOR SYSTEM

1. INPUT AMPLIFIER

Video in from the front panel attenuator switch at normal amplitude, 0.5V p-p is ac coupled to emitter follower TR600. Since this stage has a high input impedance, the 75Ω termination for the input attenuator is provided by R603, R604 and R608 on the front panel switch. The video signal from TR600 emitter passes to the amplifier, TR607, TR608 and TR609. TR607 and TR608 form a long-tailed pair and TR609 is an emitter follower. Negative feedback is taken from TR609 emitter to TR608 base and the gain of the amplifier (about x6) is determined by the ratios of R649 and R650. Frequency response is controlled by the tuned circuit, L601, C614, C615 and filter, R653, C616. These components provide a progressive roll-off starting at 1.5MHz, with a notch at 4.4MHz. The amplifier is biased so that a certain amount of white-level clipping may occur.

2. CLAMP PULSE GENERATOR

Transistor, TR611, is fed composite sync, via the emitter-follower TR610, and functions as a sync separator. The sync pulses developed at TR611 may contain sound pulses (if a Sound-in-Sync signal is used). These extra pulses are removed by the action of TR615 which is driven into conduction during the sound-pulse period by a signal derived from the digit-blanking generator, IC603b, via inverter, TR625. The blanked sync pulses appearing at the collector of TR615 are differentiated by C621 and the negative-going edges are used to drive TR614 into cut-off. Thus the required positive-going clamp pulses timed to the Back Porch Period are developed at TR614 collector.

3. START-UP CLAMP

The output of the input amplifier is passed via emitter-follower, TR612, and ac coupled to the 'start-up' clamp, TR613. Positive-going pulses of duration approximately 2μs are applied to the gate of TR613, this causes it to conduct and clamp the signal to earth potential. Clamping occurs at black level during the Back Porch. The function of this clamp is to ensure that the main clamp locks initially to the correct part of waveform. The main clamp relies on an output signal from the complete sync separator and after start-up provides the major part of the clamping action.

4. MAIN CLAMP

The main clamp follows on from the start-up clamp, TR613, the signal is passed via C619 and R663 to the emitter-follower, TR618. The FET, TR619, is turned on by a positive-going pulse on its gate. This causes the video signal to be clamped to zero volts during the Back Porch. The main clamp pulses are derived from the comparator, IC602, via inverter, TR624. Line sync pulses are inverted by TR624 and then differentiated by C635. Negative spikes from the back edge of syncs are then used to turn TR616 off so as to produce a positive-going clamp pulse at its collector and so switch on FET, TR619, during the Back Porch.

5. SYNC SEPARATION

The clamped video present at TR618 emitter may contain sound pulses in the sync-period (with a Sound-in-Sync signal). These sound pulses are removed by the action of TR621 before sync slicing takes place. During line-sync periods TR621 is driven into conduction by a positive-going pulse obtained from the digit-blanking generator, IC603b, and the sound pulses so gated out. Because TR621 continues to operate during the field blanking period alternate equalising pulses are increased in duration to 4μs.

Integrated circuit, IC602, is a differential comparator which functions as a sync slicer. The device compares the sync-pulse amplitude of the clamped video signal with a dc reference signal which has half the amplitude of syncs and is derived from the sync-level detector. When the input syncs on pin 2 go more negative than the reference level on pin 3, the output on pin 7 goes negative and thus negative-going sync pulses with a peak-to-peak amplitude of 3.5V are developed. These pulses are fed via a buffer, IC601b and c, to the mixed sync output of the sync separator, and to the 'SYNC' front panel monitor point via R643.

6. SYNC-LEVEL DETECTOR

The clamped video from the emitter follower, TR618, is fed to TR617. This transistor conducts during sync pulse periods and charges C625 to a potential proportional to the peak sync-pulse amplitude. Smoothing is carried out by R673 and C624. The emitter follower, TR620, removes the base emitter offset caused by TR617. The resultant dc signal is then fed, via a potential divider network, R676, R677, which reduces it to half sync amplitude, to the sync slicer, IC602.

7. DIGIT BLANKING GENERATOR

Separated sync pulses from IC602 are fed via a buffer, IC601, to the input of a monostable, IC603A. The time constant of IC603A is approximately 50μs. This is longer than half a television line and so prevents the generation of unnecessary blanking pulses at twice-line frequency during the field-sync period. The monostable triggers on the leading edge of syncs.

The output of monostable IC603a at pin 7 is then fed to monostable IC603b, pin 11. This monstable generates line-frequency pulses with a duration of 4.5μs. These pulses are used as digit-blanking pulses (from pin 10 via TR621) and after inversion by TR625 as the main clamp pulses.

8. FIELD-PULSE SEPARATION

Negative-going mixed sync pulses from IC601c, pin 6, are fed to the base of TR626 via R691 and C637. The time-constant of C637, R692, is so arranged that the line-sync pulses do not affect the cut-off state of TR626. However, during the longer duration broad pulses in the field synchronising period, C637 charges sufficiently through R692 to turn on TR626 on the narrow (2.3μs) line sync pulses which follow the broad pulses. The negative-going pulses on TR626 collector charge capacitor C638 such that the first pulse at IC601d input, pin 9, is the largest in amplitude. This is because successive pulses must await the discharge period of C638 via R693 before further charge can be transferred to IC601d. The output of IC601d is a positive-going 2.3μs (approx.) pulse corresponding to the gap between the first and second broad pulse.

9. FIELD IDENTIFICATION

The field pulse at IC601d, pin 8, occurs once on each field, during the narrow-line sync pulse period between the first and second broad field sync pulses. IC603a produces a 50μs pulse at pins 6 and 7 commencing at the leading edge of each line sync pulse. Since the phasing of the first broad pulse shifts by half a line (32μs) on alternate fields, the 50μs positive-going Q output of IC603a, pin 6, will only coincide with the field pulse derived from IC601d, pin 8, on EVEN fields. Similarly, the Q output of IC603a at pin 7 will only coincide with the derived field pulse on ODD fields. The AND gates, IC605d and IC605c, detect the coincidences and produce negative-going pulses corresponding to Field 1 (EVEN) and Field 2 (ODD). (See waveforms, Fig. 12.)

10. GENERATION OF LINE RATE CLOCKING SIGNALS FOR COUNTERS

The 50μs square wave signal from IC603a, pin 6, is fed to IC617b which is a monostable triggering on the negative edges of the incoming square wave and so producing 5μs wide pulses to its output. The position of these pulses relative to the incoming video is about 50μs after the leading edge of the line sync pulses. A positive-going pulse output from this monostable is fed to IC606, pin 14, to provide the decade counter with positive clock edges. The negative-going pulse output from IC617b, pin 9, is taken to the 625 line counter, IC607, and the latch, IC608c, which operate on negative clock edges.

4.16 VIDEO SIGNAL SYSTEM

1. INPUT ATTENUATOR

The 'video in' from the front panel BNC socket passes to a 3-way input attenuator switch, S606, each sensitivity position is capable of input level variations of ±6dB. For a normal input level of 1V p-p the attenuator switch selects a 6dB pad formed from R600, R601 and R602, the 75 ohms termination for the pad is R603, R604 and R608. This gives an input impedance to the unit of

75 ohms irrespective of attenuator switch setting. The 2V input sensitivity setting is selected using the 12dB pad, R605, R606 and R607. The 0.5V sensitivity setting is a direct feed from the input socket to the termination (R603, R604, R608).

The signal feed to the clamp circuit is at a nominal level of 0.5V p-p and is ac coupled from the input termination.

The 'clamp out' signal to the display switch, S601, is taken from the junction of R603, R604 at a nominal level of 0.25V p-p. A small amount of frequency compensation is provided by the capacitor C611 shunting R604.

2. SIGNAL CLAMP

The input to the signal clamp is ac coupled from the input attenuator to the emitter follower, TR600, at a nominal level of 0.5V p-p. The signal then passes to a clamp utilising a dual FET, TR601 and TR602. These are connected in a totem pole configuration with TR602 acting as a constant current source for the source follower, TR601, which provides a low impedance input at the base of TR603. This potential is adjustable by means of R617, the 'set clamp dc' preset control. Black level clamping at a time corresponding to the CSC. burst occurs at TR601 gate due to the action of TR606. The FET, TR606, is turned on by positive-going time rate pulse derived from monostable IC600a and which is triggered by the back edge of mixed sync pulses from pin 6 of IC601c. The chrominance information is maintained during clamping by the tuned circuit L602, C606, C607. This is tuned to colour subcarrier frequency by adjustment of C606.

3. OUTPUT AMPLIFIER

The clamped output is passed to the output amplifier, TR603, TR604, TR605. This consists of a long-tailed pair followed by an emitter follower, TR605. Feedback is taken from TR605 emitter to the base of TR604 via R627 and R626. The gain can be preset by R628 with C605 compensating for the frequency response. Choice of R625 enables the output dc potential at TR605 emitter to be set to 0V.

The clamped signal output at TR605 emitter is at a nominal level of 1V p-p. This signal is fed to the video amplifier comprising TR633, TR634 and TR636, which modulates the crt via the Z mod input socket. A portion of the signal at TR605 emitter is attenuated by R632, R635 to give a 0.25V p-p signal which is fed to the 3-way DISPLAY SELECT switch, S601, and then to the 'video out' front panel BNC socket via the 'CAL' push button switch, S603.

4. VIDEO OUTPUT

The 'video out' BNC socket is coupled normally via a short cable to the high impedance CH2 input of the oscilloscope. The input coupling should be set to dc and the sensitivity to 50mV/div. The signal at the 'video out' socket is at nominal level 0.25V p-p which gives a 5 division vertical display on the oscilloscope.

When the 'CAL' button is operated a 0.25V p-p square wave appears on the display. This should correspond to the same amplitude as obtained from a 1V p-p video signal when the video attenuator is switched to 1V (0dB) position. If the display function switch, S601, is switched to 'Picture' a field ramp waveform is routed to the display and at the same time a line-rate ramp replaces the normal X-deflection timebase output. This produces a 625-line raster on the oscilloscope.

4.17 TV TRIGGERING SYSTEM

1. TV TRIGGER SELECTION AND DELAY

TV triggering is controlled by means of a 12-way front panel Line selection switch, S602, and the main Trigger Select switch, S40. This latter can be set to 'TV' or 'TV DELAY' corresponding to a fixed trigger point just prior to the leading edge of TV sync pulses or to a variable delay trigger controlled by the multi-turn 'DELAY' potentiometer.

The trigger signal from the Line selector switch, S602, is routed to pin 4 of monostable IC617, which triggers on positive edges. The time constant is variable between approximately 4μs and 90μs by means of the 'DELAY' control. R714, pin 7, of the monostable is taken via the 'TRIGGER SELECT' switch, S40, to the trigger input of the timebase, via the attenuator R725, R577. (R577 is mounted on the Trig Select switch.) Pin 6 of the monostable goes to TR635 via R749 to provide bright-up on the raster display, thus indicating the position of the DELAY control in PICTURE mode.

2. 625 LINE COUNTER

IC607 is a twelve stage binary counter (2 stages are not used). In all positions of the LINE SELECT switch except where the LINE COUNTER is used IC607 is reset to zero by the EVEN field (F1) pulse. (See section 4.15.9 on field identification.) This pulse is fed from pin 11 of IC605d and inverted by IC605b to provide a narrow positive-going pulse to the NOR gate, IC616a. Because the line counter is not selected R711 pulls IC616b and d inputs high, thus generating a logical low on IC616b, pin 4, and IC616d, pin 11. The pulse therefore becomes inverted by IC616a and again by IC616c to provide a positive-going pulse to reset IC607. The counter is clocked by the leading negative-going edges of line rate pulses from IC617, pin 9, and counts from 0 to 625.

3. FIELD TRIGGERING (EVEN FIELDS, ODD FIELDS OR BOTH)

The trigger signals are taken to the DELAY monostable, IC617, via the LINE SELECT switch, S602. 'EVEN FIELD' trigger pulses come from IC605b, pin 4; these are positive-going, and coincident with the gap between the first and second broad pulse during Line 1. The ODD FIELD trigger pulses come from IC605a, pin 3, and are similar to the EVEN FIELD pulses but occurring during line 314.

BOTH FIELDS triggering is derived from the Field pulse separator system using the positive pulse output from IC601, pin 8. (See section 4.15.8 on field separation.)

4. LINE REP TRIGGERING

LINE REPETITIVE triggering actually operates on alternate lines and the signal is derived from the 625 line

counter, IC607. In this mode the counter is reset by the EVEN field pulse from IC616c, pin 10. The LINE REP trigger pulse consists of the Q1 output of the counter, IC607, pin 9, which effectively divides the line frequency by two, so providing trigger on every other line. This enables the DELAY control to take up more than one line period of delay, providing an overlap into the next line if required.

LINE REP triggering may be used on a generator without field sync information, and under these conditions, the counter, IC607, receives no reset pulse but simply works as a divider.

5. LINE PAIR TRIGGERING

The 625 line counter is reset as usual in this mode by the EVEN field pulse from IC616, pin 10. The specified line pairs on the LINE SELECT switch begin from lines 16 and 329 and finish with lines 22 and 335. IC609c, IC609a, together with IC615d which is connected as an inverter, form a 5 input NAND gate. The output at pin 9 of IC609a will be low when Q9, Q7, Q3, Q2 and Q1 outputs on IC607 are all high, corresponding to the binary code 101000111 = 327. Similarly, IC609b will be low when the code 1110 = 14 is reached, corresponding to high outputs on Q4, Q3 and Q2. The outputs from IC609a and IC609b go to IC610d, IC610c and IC610b, IC610a, respectively, which are connected as flip-flops. The purpose of these is to prevent further spurious outputs from IC609a and b after the required codes of 327 and 14 have been reached. For example, IC609a could give another output for 10100$\underline{1}$111 (=335) since the extra Q4 digit from IC607 would not be detected.

The negative-going signal at the output pin 11 of IC605d corresponding to the EVEN field pulse is applied to pin 1 of the flip-flop IC610a/b. This sets the output of IC610a, pin 3, high and since IC609b, pin 6, will normally be in a high state, IC610b, pin 14, output of the flip-flop will be low. When the count of 14 lines has occurred IC609b goes low, thus sending the flip-flop output IC610b, pin 14, high. The output will remain high until the next frame pulse, whereupon the flip-flop is reset.

A similar situation exists with the output of IC609a, pin 9, and the flip-flop IC610c/d, except that this flip-flop is reset by the ODD field pulses (line 314) from IC605c, pin 10. Assuming that one field has already occurred, then the flip-flop IC610c/d will be giving a high output at pin 10 into IC615c. When the count 14 is reached IC610b, pin 14, goes high, driving IC615c, pin 10, low, and thus removing the reset from IC606. IC606 is a decade counter which is clocked by the positive-going edges of the line frequency output pulses from IC617b, pin 10. On the 15th line count Q1 of IC606, pin 2, goes high and gives a trigger pulse to the LINE SELECT switch. If this switch has been set to view the line pairs 16/329, then the monostable, IC617a, will be thus activated giving trigger signals to the A timebase just before line 16 occurs. Lines 17 – 22 are triggered by selecting the switch positions Q2 – Q7 on the counter IC606. When the counter has received 9 clock pulses from IC617 output Q9, pin 11, goes high, thus driving the CLOCK ENABLE high and preventing the counter recycling. It then awaits the reset pulse from IC610c/d via IC615c when that bistable is clocked by the ODD field pulse from IC605c. The process then repeats for the lines 329 – 335 in the ODD field, when IC609a, pin 9, goes low on line 327.

6. LINE SELECTOR

When this mode is selected by the LINE SELECTION switch, the trigger point of the timebase is controlled by the 'UP' and 'DOWN' push button switches, with the LED display indicating the line selected. IC607 functions as a free running 625 line counter. It is not synchronised by the detected Field Sync pulse. When the UP push button is selected the count changes to 626, and when the DOWN button is pushed the count becomes 624. This shifts the phase of the 625 line counter by one step with respect to the incoming 625 line video signal, incrementing or decrementing the chosen line. The normal 625 count is detected by IC611a, IC611b and IC612b, which function as a 5 input AND gate working on the signals Q1, Q5, Q6, Q7 and Q10. This corresponds to the binary code 1001110001 or 625. If neither of the 'UP' or 'DOWN' push buttons, S604 or S605, are pressed the inputs (pins 12, 13) to IC614d are high so its output at pin 11 will be low. Consequently IC614c output at pin 10 inserts a high input to pin 1 of IC614a. In addition, the decade counter, IC618 and IC619, are held reset by the high output from IC615b (pin 4). This is due to the low gate output from IC615a which has its inputs held high by the pull-up resistors, R709 and R710. The clock enable input and the Q2, Q4 outputs from IC618 and IC619 will both be low, thus making IC608d output high at pin 11. The gates, IC613b, IC613d, IC614b and IC614a, therefore allow the Q1 signal from IC607, pin 9, to travel through them unimpeded, to emerge at IC614a, pin 3, thus setting up the Q1 condition at the gate, IC611a, as described previously.

The detected 625 count from IC612b, pin 4, then proceeds to the gate system, IC616a, b, c and d. This functions as a switch operated by the LINE SELECTION switch either to gate the detected field pulse to reset IC607, or in this case where the LINE SELECTOR function is required to gate in the 625 count. In this position of the switch, the pull-up resistor, R711, is held low making the output from IC616b, pin 4, high. This in turn makes IC616a output low at pin 3 and prevents the Field pulse input at pin 1 from travelling through the gate. As a result, the detected 625 line count incurs a double inversion by gates IC616d and IC616c and emerges at pin 10 to reset the counter IC607 at pin 11.

Another gate system consisting of IC611b, IC611c and IC612a functions as a four input AND gate, with the output from IC611b being used again, and IC611c detecting Q5 and Q6 from IC607. The total count being Q10, Q7, Q6, Q5 corresponding to the binary code 1001110000 or 624. This provides positive trigger pulse output from IC612a, pin 3, to operate the monostable, IC617a, via the

LINE SELECT switch. The count arrives before the 625th line rest pulst in order to give early timebase trigger.

7. ADJUSTMENT OF LINE COUNT BY 'UP' AND 'DOWN' SWITCHES

When the DOWN push button, S605, is pressed the input pin 2 to the NAND gate, IC615a, is brought low (normally this input is held high by the pull-up resistor, R710). As a result IC615a output on pin 3 goes high, driving the inverter, IC615b, output low at pin 4. This removes the resets on the decade counters, IC618 and IC619. These counters are clocked each time a reset pulse enters IC607; hence they are effectively counting the number of elapsed Fields. After IC607 has counted 625 twice, Q2 of IC618 goes high driving the output of IC608d, pin 11, low. The output from IC613d, pin 11, will therefore maintain a high state thus blocking the Q1 output of IC607 from passing through the gate. The pull-up resistor, R709, is not grounded and holds the inputs to gate IC614d and pin 5 of IC614b high. As a result IC614b output at pin 4 will be low and therefore IC614a output on pin 3 will be high. This sets a '1' input in IC611a, pin 8, and makes the Line counter reset combination IC611b, IC611a and IC612b count to 624, corresponding to the inputs Q10, Q7, Q6 and Q5. As the third reset pulse enters IC607 the Q2 output from IC618 drops low again, allowing the Q1 output from IC607 to pass through the gates IC613b, IC613d, IC614b and IC614a to reset IC607 on the 625th count in the normal manner. The counter, IC607, continues to count 625 until Q2 goes high again and a count of 624 occurs once more. When IC618 has cycled 4 times, (i.e. 40 counts) Q4 on IC619 goes high, holding the input to IC608d, pin 13, high and preventing further clocking occurring in IC618 and IC619 by holding the CLOCK ENABLE inputs high. As a result, IC607 is made to continuously count to 624. The purpose of this sequence is firstly to prevent contact bounce on the UP/DOWN push buttons from upsetting the count by allowing two Fields to occur before any count up or down takes place. This is effected by using the Q2 output of IC618. Secondly, for the first four digit changes on the LINE SELECTOR display, the numbers only change every 10 Fields, allowing the numbers to move slowly. If either of the buttons are held in, the counters, IC618 and IC619, latch and make the count settle on either 624 or 626, according to whether the DOWN or UP button is selected, thus allowing more rapid number change.

Selection of the UP push button (S604) grounds the pull-up resistor, R709. This makes the output from gate IC615b low and the counters, IC618 and IC619, operate in the way described previously. When either Q2 on IC618 or Q4 on IC619 is high, then the output of IC608d is low. The output of gate IC613d is high (pin 11), holding the input high to gate IC613a on pin 1. This allows the Q2 count from IC607, pin 2, to proceed through the gates IC612d, ID612c, IC613a and IC613c. Because R709 input to IC614d, pins 12 and 13, is held low, its output at pin 11 is high, and also the output of IC614b, pin 4, will be high thus allowing the signal for the Q2 count to pass through the gates IC614c and IC614a. This makes the counter reset combination IC611a, IC611b and IC612b count to 626. The input code set up will be Q10, Q7, Q6, Q5 and Q2 representing the binary number 1001110010 on counter IC607.

8. LINE SELECTOR DISPLAY

The LED display, IC621, indicates the line selected and is controlled by the counter/latch, IC620. A positive-going EVEN FIELD pulse from IC605b, pin 4, resets the display counter/latch, IC620, and the flip-flop comprising IC608a and IC608b. This pulse occurs half way along line 1, corresponding to the position of the narrow equalising pulse. When the flip-flop is reset, IC608b drops low at pin 4 enabling the NOR gate, IC608c, to operate on the line rate pulses from IC617b, pin 9. These pulses are about 5μs wide, have a negative leading edge and occur approximately 50μs after the leading edges of line sync signals. Thus IC620 is clocked by positive edge signals from IC608c, pin 10. When the 625 line counter, IC607, resets, the pulse is also conveyed to the flip-flop, IC608a and IC608b, which resets and prevents further clocking of IC620. In addition, the LATCH ENABLE goes high, thus holding the contents of the LATCH and allowing the display to show the recorded count.

4.18 PICTURE OPERATION

When 'PICTURE' display is selected the DISPLAY SELECT switch, S601, provides a +24 volt supply to the Line and Field ramp generator circuits and also to the Picture Drive output amplifier. This supply is derived from the 190 volt rail supply using the dropper resistors, R742, R743, and the zener diode, D610.

1. LINE RAMP GENERATOR

Line-rate pulses from IC603b, pin 9, are used to switch TR638 via C673 and R761, which discharges C674. TR639 is a constant current generator which charges C674 thus producing a line ramp at TR640 base. The resistor R759 is used to adjust the ramp amplitude. The emitter follower, TR640, feeds the dc restorer circuit, C675 and D613, and from there the ramp is connected to the x amplifier via the diode gate, D614, D615 and R767. (The wiring arrangement conveys the gated timebase ramp to the 'TV' timebase board before going to the x output amplifier via pin 12 on the output socket PLB.)

2. FIELD RAMP GENERATOR

Positive-going Field sync pulses from IC601d, pin 8, go to the Monostable IC600b, pin 12, which triggers on the leading edges and gives negative edge pulses of approximately 150μs duration at pin 9. This signal is used to charge C664 via R750 and the base emitter diode of TR637. TR637 is therefore switched on and discharges C665. At the end of the input pulse, R752 discharges C664, but not sufficiently to allow TR637 to turn on before the next input pulse arrives. Thus R752 effectively defines the base current of TR637. When C665 has been discharged by TR637 during the brief 150μs period, R753

and R758 provide an approximately constant current to charge C665 up again. A 2.5V ramp exists at the collector of TR637 which is attenuated by R758 and R753 to about 350mV and buffered by TR641 to provide the vertical Field ramp into the Y-amplifier. The signal is coupled by C668 to R754 and R755 which provide a dc bias on the ramp to centre the picture on the screen when the clamp amplifier is in use.

The DISPLAY SWITCH, S601b, connects the Field ramp to the Y amplifier input, via the BNC output socket on the front panel.

3. PICTURE DRIVE AMPLIFIER

A positive-going video signal of 1V peak-to-peak amplitude is fed from the clamp amplifier output (emitter of TR605) to the picture Drive amplifier input at TR633 base via the capacitor C657. TR633 is biased by R730 and R731 and acts as a direct coupled emitter follower into the common emitter amplifier, TR634. The output of TR634 is buffered by the emitter follower, TR636, to provide a negative-going video output of approximately 9 volts amplitude. HF peaking is provided by the network R734 and C658. TR635 is switched by the positive signal from the trigger monostable, IC617a, pin 6, via R749 to provide bright-up on the picture to indicate the monostable trigger position.

After being fed through C659, the video output from TR636 is clamped at sync tips by D609 and the zener D620, to bias the modulation amplifier to the necessary level for handling the waveform. The video signal is connected to the rear panel PICTURE DRIVE output socket via L603 and R744.

4.19 EXTERNAL X AMPLIFIER

The circuit for the external X amplifier is included on the 'TV' logic circuit board. The external input signal is applied to the base of the amplifier transistor, TR647, through the capacitor/resistor network, C683, R791. The trimmer, C684, is used to set the HF response. The diode, D618, protects the base-emitter function of the transistor against excessive reverse voltage. Resistors, R790, R791 and R792, set the quiescent base voltage of the input transistor. Capacitor, C682, provides some HF peaking. The collector voltage swing is passed via the emitter-follower, TR648, through the diode, D619 (when the circuit is enabled), to the X amplifier. When External X is selected on the timebase range switch (S43) a +15V supply is sent to the DISPLAY SELECT switch (S601e). If this switch is not in 'PICTURE' mode, then the +15V supply is used to power the supply rail of the External X amplifier. When the amplifier operation is not selected R769 pulls this rail down to −15V to shut off the circuit.

4.20 X GATE AND X OUTPUT AMPLIFIER

The input of the X output amplifier can be connected to the timebase, the 'TV' ramp outputs or the output of the External X amplifier, as determined by the DISPLAY SELECT switch (S601),and the timebase range switch, S43. The switching is performed by diode gates D432/D433 and D614/D615 for the timebase and TV line ramps respectively, and by D619 for the External X amplifier.

When External X is selected, and the DISPLAY SELECT switch, S601, is in either the 'CLAMP' or 'CLAMP OUT' mode, −15V is fed via S601C to R767 to cut off the gate comprising D614/D615. A second −15V supply via S601d cuts off the timebase gate D432/D433 via R549. The External X amplifier is then enabled by a +15V supply fed via S601e. Output from D619 is then fed to the X output amplifier.

When the timebase range switch is in any position other than Ext X, S601c and S601d, determines whether the TV line ramp or the timebase ramp is gated to the X output amplifier by applying +15V to either R767 or R549. R766 and R548 keep either gate off in absence of this voltage. Note that if Ext X is selected when the DISPLAY SELECT switch is in PICTURE mode, then the PICTURE mode is operative, since the Ext X +15V supply from S601e is not present. The X output amplifier consists of a long-tailed input pair (TR921 and TR929) driven from the current source, TR923. The inputs to the amplifier are the selected ramp/Ext X signal to the base of TR921 and the shift voltage to TR929. The output from this pair feeds via the emitter followers, TR922 and TR928, into the differential cascode output stage. There is overall shunt feedback to set the gain and stabilise the working conditions through resistors R923 and R949. The gain of the amplifier is set by the network, R927, and the preset R933, in the X1 mode. In the X10 mode the relay, RL921, is energised and contacts bring R938 and preset R943 into circuit.

4.21 CALIBRATOR

The components forming the calibrator circuit are mounted on the TV logic PC assy. The circuit consists of an emitter coupled multivibrator, TR644, and TR645, with C677 as the timing capacitor. The collector current through TR645 is used to turn on TR646 which supplies a switched current to a 6.2V reference zener via R779. The square waveform on the cathode of the zener is attenuated by the resistor chain R786, R787, R777 and R778. The potential formed across R777 and R778 is 1 volt peak-to-peak which is conveyed to the front panel output pin. The potential across R778 is 250mV peak-to-peak, which is switched by push button S603 to provide the TV calibration source.

4.22 THE BRIGHT-UP AMPLIFIER

The Bright-up amplifier which controls the Z modulation of the crt consists of an inverting amplifier, TR970, TR971 and TR972, with shunt feedback applied through R977, the base of TR970 being a virtual earth point. The inputs include current pulses from the timebase bistable via TR421, chop blanking current pulses from TR218, and external Z modulation current waveforms (from emitter-follower, TR903 and R974), a dc current derived from the INTENSITY control, R60, through R970, and

a bias current through R971, obtained from the timebase DISPLAY switch circuit via R776, D612. The instantaneous sum of these input currents is balanced by the feedback current from the output through R977, so that the output voltage waveform follows the sum of the input currents.

The Intensity control current and the Ext Z modulation current are added through D970, the maximum intensity condition being when the current in D970 is zero, and the blanked condition being when the current in D970 is +2mA.

During the chop blanking period, a further +2mA current pulse is added which makes total applied input current $\geqslant$+2mA, and blanks the trace for all settings of the intensity control.

The maximum output from the amplifier is approximately 60 volts, corresponding to this 2mA change in input current. The diode, D971, ensures that when the amplifier is overloaded by a negative input, bright-up inputs do not move far from their normal working voltage.

Diodes, D974 and D975, ensure that TR972 does not bottom. TR971 provides essentially a high impedance constant current load for TR972 but C974 causes it to act as a complementary amplifier with TR972, to provide a low output impedance at high frequencies to drive the mainly capacitive load.

The output of the amplifier is connected via C979 directly to the grid of the crt, and through R982 to the low voltage end of the grid supply voltage doubler. The dc voltage with respect to ground applied to the grid, is then determined by the potentiometer, R988 (to allow for variations in grid cut-off between crt's), resistor, R987, across grid supply and the voltage on the output of the amplifier.

4.22.1 BEAM CURRENT LIMIT

Due to the high tube EHT used it is necessary to limit the crt beam current to prevent burning of the phosphor when the spot is stationary. Transistor TR904 is normally held on via R954 when no beam current is present, hence the emitter of TR905 is close to ground and no current is fed into the bright-up amplifier. The return current for the EHT multiplier flows through R954, as the intensity control is advanced TR904 is turned off, TR905 conducts feeding current to the bright-up amplifier, restricting the drive to the tube crt grid and limiting the beam current to approx. 1.5μA.

Under normal timebase operation when a ramp is present, diodes D904, D905 and C909 provide a positive bias to TR904, overriding the beam current limiting.

4.23 THE POWER SUPPLIES

The OS3350 basically operates from positive and negative 15V lines and a +190V line, each stabilised and independently protected against overload. The EHT lines are all obtained from a high frequency oscillator with overload protection but with direct stabilisation only on the −2kV crt cathode supply. This oscillator is supplied from the +20V unstabilised line used for the +15V line.

All supplies are obtained from transformer, T83, via the range selector switch, S81, the supply fuse, FS83, and supply on/off switch, S80.

One secondary from T83 is the 6.3V supply to the crt heater and another the low voltage (approx. .25 volt) for the line trigger signal. This latter voltage passes via SKB − PLB19 and PLB20 to the trigger selector switch. The three remaining secondaries are rectified and smoothed as follows.

4.23.1 +15V, −15 V and +190V LINES

One secondary from T83 feeds the bridge rectifier, MR83, and develops approximately 20V across capacitor, C85. This is used to obtain a stable, overload protected, −15 volt line using an integrated circuit regulator, IC801, which contains a reference, comparator input amplifier and output current amplifier. In addition it includes the overload protection circuitry to operate from the voltage developed across the current sensing resistor, R836. The output from this IC regulator drives the external series regulator, TR838.

The output of the line is set to be −15V by the preset potentiometer, R838. Components, R855 and C831, reduce the noise present on the internal reference and C832 gives feedback compensation to prevent oscillation.

A similar secondary from T83 is rectified by MR82 and develops approximately +20V across C84. Protected by FS832 this +20V supply feeds the EHT oscillator. The voltage across C84 is also used to obtain the stabilised +15 volt line.

TR833, TR834, TR835 and TR837 form the +15V stabiliser circuit, which is referenced to the −15V line. If the +15V line is not at the correct potential, the junction of the two equal resistors, R847 and R848, will not be at 0V. The resultant differential voltage between the bases of TR833 and TR834 will modify the collector current of TR833 to drive through TR835 to the series regulator element, TR837, and so correct the line potential.

Excessive current drawn from the +15V line will develop a potential across R835 causing D833 to conduct in turn limiting the base current to TR835 and so also that in TR837.

Fuses, FS833 and FS834, protect the +15 and −15 volt lines respectively.

Protection diodes, D835 and D836, are normally reverse biased and only conduct in the accidental condition of a short circuit between the +15V and −15V lines.

Diode, D834, protects the base-emitter junctions of TR833 and TR834 against excessive reverse voltages. Capacitors, C836 and C833, give hf roll-off to prevent oscillation; C835 reduces output ripple.

The secondary from T83 is rectified by MR81 and develops approximately 220V across C83.

R84 and C86 reduce the output line ripple. The +190 volt line is referenced from the −15 volt line by resistors, R842 and R843. Any error potential at the junction of these resistors drives the error amplifier, TR831, which in turn controls the series transistor, TR839. Transistor, TR832, protects TR839 from over voltage at switch-on, or in the event of failure of the −15V line. If the junction of the potential divider, R840 and R841, goes too far negative, TR832 conducts, allowing TR839 to conduct.

Short circuit protection on the 190V line is by means of the fuse, FS831.

4.23.2 EHT SUPPLIES

The EHT supply circuitry is as shown in Fig. 8. It comprises a single transistor, transformer coupled oscillator with a single tapped secondary to provide three lines of approximately −2000 volts, −2100 volts and +14kV, mounted together with an error amplifier within the EHT box assembly.

The tap on the transformer secondary feeds two voltage doubler circuits, that for the grid supply being formed by D804, D806 and C804, C805. The return path for the doubler circuit is via TR802. This transistor is driven from the bright-up amplifier and modulates the grid supply at dc and low frequencies. High frequencies are fed to the grid of the tube via C979. The second voltage doubler, D802, D803 and C802, C803, feeds the crt cathode via the 120V zener, this ensures that the grid is at least 120V more negative than the cathode, the actual value being set by R988 and allows for variations in crt cut-off voltage. The cathode supply voltage doubler return is via R816. Excessive tube cathode current turns TR805 on and reduces the drive to the crt. This effectively limits the available tube beam current and gives over-current protection to the oscillator (see also section 4.22.1). EHT stabilisation is achieved by feeding a small fraction of the cathode voltage to the error amplifier, TR803 and TR804, via R805 where it is compared with a feed from the stabilised +15 volt line on the power supply board. Transistor, TR803, varies the base drive to TR801 so controlling the collector voltage and hence the dc output.

Additional over-current protection is provided by sensing the voltage drop across L801 against D808; this limits the maximum available drive to the base of the oscillator transistor, TR801, and hence its maximum collector current to approximately 600mA. If this current is maintained the fuse, FS832, will blow.

Adjustment of the EHT is by R854 "Set EHT" mounted on the power supply printed circuit board.

The full output from the transformer secondary is taken to a six stage multiplier module to provide +14kV for the final anode of the crt.

4.24 CATHODE RAY TUBE AND ITS INPUTS

The OS3350 employs a conventional mesh p.d.a. tube with a high efficiency aluminised screen.

The interconnection diagram, Fig. 9, shows the necessary connections to the various electrodes.

THE GUN

An independent winding on the mains transformer drives the heater for the cathode. The beam current and hence the spot intensity is controlled by the differential potential between the grid and cathode. The −2kV potential is the direct stabilised output from the EHT oscillator. The grid potential is the sum grid supply from the EHT oscillator and the output potential of the bright-up amplifier to which the grid supply is referred.

The crt beam is brough to a clear, well focussed spot by varying the potentials applied to the focus and astigmatism electrodes. These signals are derived from R82 (focus) and R81 (astigmatism) mounted on the front panel, the latter being a screwdriver adjustment. The focus electrode is normally variable over the range −530V to −740V and the astigmatism from +120V to 0V.

THE DEFLECTION SYSTEM

The Y plates are connected to the output of the Y amplifier and the differential signal applied, deflects the beam in the vertical direction. The mean plate potential is normally +75V and the sensitivity is approx. 5.2V/cm.

Similarly, the X plates are connected to the X output amplifier and the differential signal deflects the beam in the horizontal direction. The mean X plate potential is normally +95V and the sensitivity is approx. 16.6V/cm.

The deflection plate shield, S1, screens the deflection plates from the other electrodes and is held at a potential of +65V obtained from the junction of R919 and R920 on the interconnect p.c.b.

The interplate shield, S2, screens the X plates from the Y plates and is held at a potential 15V more negative than the X mean plate potential, derived from the wiper of R381 on the Y output p.c.b.

Having passed through the deflection plate system the beam accelerates to the screen which is held at +16kV relative to cathode by an output from the EHT oscillator, striking the phosphor at high velocity to produce the necessary bright trace.

THE TRACE ROTATION COIL

A coil, L83, fitted round the neck of crt, inside the magnetic shield is used to align the trace with the horizontal graticule lines.

The current for this coil is taken from the front panel potentiometer, R83 through R849, on the power supply board.

4.25 SCALE ILLUMINATION

The external scale is illuminated by two lamps, ILP83 and ILP84.

The supply for these lamps is derived from the emitter-follower, TR836, on the power supply board; being set by the scale illumination potentiometer, R80, on the front panel.

Both the emitter-follower and the control potentiometer are supplied from the full-wave rectified signal taken from the transformer at the junction of diodes, D83 and D84.

4.26 THE BEAM FINDER

Operation of the TRACE LOCATE push button performs the following functions.

Firstly, R85 is connected in a series with the +190 volt line that feeds the X and Y plate amplifiers. This limits the swing to approximately 8cm in the X direction and 12cm in the Y. To further limit the scan in the Y direction to 6cm, the current in the output stage is reduced by switching R366 in series with the normal emitter resistor of the current source transistor, TR355.

The Bright-Up amplifier is biased by resistors, R973 from the −15V line and R993 from the switched +190V line. The values are so arranged that 2mA flows into the amplifier input from the negative supply, allowing normal operation of the INTENSITY control. When the TRACE LOCATE button is pressed this bias current is changed, due to the voltage across R993 falling to 70V, thereby increasing the negative bias to approximately 4mA which gives full bright-up to the display, overriding the setting of the INTENSITY control.

Maintenance

Section 5

5.1 GENERAL

The instrument is electrically protected by five fuses as follows:-

1. 1A 'Slo-blo'–size 20mm (FS83 Pt.No.34790) for the 95-130V Supply ranges.
   500mA 'Slo-blo' size 30mm (FS83 Pt. No.33685) for the 190-260V Supply ranges.
2. 250mA size 20mm (FS831 Pt.No.32338) in +190V supply line and mounted on the Power Supply board.
3. 500mA size 20mm (FS832 Pt. No. 32339) in the +20V line supplying the EHT Oscillator mounted on the Power Supply board.
4. 1A size 20mm (FS833 Pt. No. 52162) in the +15V line and mounted on the Power Supply board.
5. 1A size 20mm (FS834 Pt.No.52162) in the -15V line and mounted on the Power Supply board.

Access to the four latter fuses is by removal of the bottom cover.

IMPORTANT BEFORE CHANGING FUSES

The instrument must be switched off and the mains input lead removed from the mains supply socket.

5.2 FAULTS

A faulty instrument should at all times be sent for repair to London Test Section, PE/C/QA2.3.4.1. Servicing Registry, Studd Street, in accordance with the A343 procedure as detailed in T1 E9 F0020.

Under no circumstances should a user undertake any fault location, component change or realignment, except by prior arrangement with the appropriate QA Servicing Division.

5.3 OPERATING DIFFICULTIES

In the event of any operating difficulties with the Oscilloscope No. 18A please contact THQ/NE/T5.2.3.

TR218	Collector	+2.8V
TR219 and TR220	Emitters	+6.8V
TR300 and TR301	Emitters	+4.1V
TR300 and TR301	Collectors	−1.4V
TR302 and TR303	Collectors	−2.3V
TR304 and TR305	Collectors	+3.8V
Pins 43 and 44		+2.4V

5.5 CALIBRATION PROCEDURE

5.5.1 TEST EQUIPMENT

1. Variable autotransformer. Output voltage 95 to 260V at 1A with ac rms voltmeter (Variac).
2. Digital Multimeter with 10MΩ input impedance, 4½ digit, accuracy within 0.1%.
3. High voltage probe for Digital Multimeter capable of operating up to 20kV.
4. Time Mark Generator. Marker generator of 0.1μs to 1 sec, accuracy within 1%.
5. Squarewave Generator. 1MHz flat top square wave generator with adjustable amplitude 0.1V to 1V into 50 ohms having a rise time of less than 2ns.
6. RF Sinewave Generator. 500kHz to 60MHz with 50kHz reference frequency. Output amplitude 25mV to 5V p-p into 50 ohms. Amplitude accuracy at 50kHz and 500kHz to 60MHz within 2%.
7. LF Sinewave Generator.
8. Capacitance Standardiser. 1MΩ/28pF, BNC 50Ω termination. BNC - BNC connector leads (PL43 & PL94). Timebase Extension Lead PL91. Video Z mod/Picture drive link (PL106).
9. Colour Calibrator. e.g. BBC UN2/506 10kHz square wave +4.43MHz subcarrier.
10. OFF-AIR VIDEO SOURCE (nominally 1V p-p video + sync) into 75Ω.
11. DUAL BEAM OSCILLOSCOPE (preferably with TV trigger). Sensitivity 5mV/cm: Bandwidth 10MHz.
12. Stable dc voltage source capable of supplying 50mA at 2V.

NOTE: Calibration should be carried out at normal ambient temperature and should not be commenced until the instrument has been operating for at least 15 mins.

5.5.2 SET SUPPLY RAIL VOLTAGE

1. Set the INTEN control to minimum.
2. Set the SUPPLY VOLTAGE switch on the rear panel to suit the supply. Apply the supply voltage via the Variac set to mid-range of the Supply Voltage setting.
3. Check that the SCALE control varies the scale intensity and that the neon, N80, is energised.
4. Connect the digital meter between chassis and pin '−15V' on the Power Supply printed circuit board. Adjust the voltage to −15V ±2% by means of R838.
5. Check that the voltage to chassis on the following pins on the Power Supply printed circuit board, are within the following limits:

'+15V'	+15	±4%
+190V	+190V	±4%

6. Connect a HV probe to the meter to read 2500V, and meter between chassis and pin 'VK' on Bright-Up Amplifier printed circuit board. Adjust R854 on Power Supply printed circuit board for a reading of −2000.
7. Check that EHT supply at tube cavity cap connector is 14kV ± .7kV.

5.5.3 SET TUBE CUT-OFF AND VISIBLE DELAY

Due to small changes in the crt control grid characteristics during warming up, the first part of the adjustment should be made as soon as a trace appears after switch-on.

Advance BRIGHTNESS control to the '9 o'clock' position. Adjust R988 on Bright-Up Amplifier printed circuit board so that the trace is just not visible.

Set the TIMEBASE controls such that the oscilloscope functions with CH1 or CH2 trigger and in the normal (i.e. not TV) mode. Set the Range switch to give a sweep rate of 20ns/cm. Inject the 1MHz fast rise pulse and adjust the trigger so that the leading edge is visible.

5.5.4 Z MODULATION

1. Apply a 1kHz square wave of 5V amplitude to the Z MOD socket on the rear panel and to CH1 INPUT socket with CH1 VOLTS/cm switch set to 2V.
2. Obtain a stable trace and check that the modulation is just visible.
3. Increase input to 20V p-p, check that the trace can be fully blanked and that positive signals cut off and negative signals bright up the trace.

5.5.5 ADJUST TRACE ALIGNMENT

Set Timebase to 1ms/cm and TRIGGER SELECT to FREE RUN.

Adjust R850 (Trace rotation preset) to bring the trace parallel to the horizontal centre line.

5.5.6 GEOMETRY

Apply to CH1 INPUT a 1kHz sinewave to give an amplitude of 8cm, adjust ASTIG and FOCUS controls for a sharp display and set Timebase to display approximately 10 cycles. Adjust R381 (on the Y O/P board) for a comromise between horizontal and vertical deflection to eliminate pincushion and barrel distortion. Reset ASTIG and FOCUS controls if necessary.

5.5.7 X AMPLIFIER ADJUSTMENTS

These adjustments should be carried out with the TB unit on an extension lead, PL91, to give access to controls.

1. Set TIME/cm to EXT X and VARI TIME/cm control to CALIBRATED. Also set the DISPLAY SELECT switch to either CLAMP or CLAMP OUT.
2. Inject a 10V p-p 1kHz square wave into the EXT X socket.
3. Adjust R935 on X amplifier and Bright-Up printed circuit board, to give 10cm of X deflection.
4. Pull the Fine X Shift (x5 Amp gain).
5. Inject a 2V p-p 1kHz square wave into the EXT X socket.
6. Adjust R936 on X amplifier and Bright-Up printed circuit board, to give 10cm of X deflection. Switch back to x1 amp gain.

7. Inject an 8V p-p 10kHz square wave into the EXT X socket. Adjust C684 (on TV logic printed circuit board) to remove any 'tail' which extends beyond the bright spots at the extremes of the deflection.

5.5.8 TIMEBASE ACCURACY ADJUSTMENT

These adjustments should be carried out with the Timebase operating on an extension lead, PL91, to give access to the appropriate controls.

Timebase:

1. Set TIME/cm to 1ms/cm; VARIABLE TIME/cm control to CALIBRATED.
2. Inject 1kHz marker pulses into CH1 channel and trigger for stable trace.
3. Adjust R510 on the Timebase printed circuit board for 1 marker pulse per cm.
4. Set the Timebase Range Switch to 0.1μs/cm, VARIABLE TIME/cm control to CALIBRATED.
5. Inject 10MHz marker pulses into CH1 channel and trigger for a stable trace.
6. Adjust C435 on the Timebase printed circuit board for 1 marker pulse per cm.
7. Check that TIME/cm VARIABLE gives greater than 3:1 reduction in speed.

5.5.9 TRIGGER LEVEL SLOPE BALANCE ADJUSTMENT

Adjustment to be carried out with Timebase on extension lead PL91.

1. Inject a 1kHz sine wave into CH1 and set TRIGGER LEVEL control to mid-position, Trigger Coupling in AC/TV position.
2. Adjust R453 ("slope Bal") so that there is no significant movement of the trigger point when the TRIGGER SELECT switch is moved from "+ve to −ve".
3. Move TRIGGER COUPLING to dc position and adjust R213 to obtain the same trigger point. Repeat using CH2 channel and R223.

NOTE: R213 and R223 are situated on the Delay Drive/ Beam Switch printed circuit board assembly.

5.5.10 CHANNEL 1 & 2 FINE GAIN CONTROL BALANCE

1. Set CH1 VOLTS/cm switch to 5mV, INPUT COUPLING switch to GND, Mode switch to CH1, Timebase to Free Run.
2. Set trace on centre line by means of CH1 shift control. Adjust front panel BAL control to give no trace movement when the CH1 FINE GAIN control is operated.
3. Repeat procedure for Channel 2.

5.5.11 CHANNEL 1 & 2 STEP ATTENUATOR BALANCE

1. Set CH1 VOLTS/cm switch to 20mV, INPUT COUPLING switch to GND, Mode switch to CH1, Timebase to Free Run.
2. Set trace on centre line by means of CH1 SHIFT CONTROL. Adjust Step Bal (CH1) to give no trace movement when the VOLT/cm switch is moved to 5mV/cm.
3. Repeat procedure for Channel 2, adjusting Step Bal (CH2).

5.5.12 X5 GAIN BALANCE/INVER BAL (CH2)

1. Set CH1 VOLTS/cm switch to 5mV INPUT COUPLING switch to GND, Mode switch to Y1, Timebase to Free Run.
2. Set trace on centre scale line by means of CH1 shift control. Adjust R146 (CH1) so that no trace shift occurs when the X5 pull switch is operated.

5.5.13 DELAY LINE MATCHING

1. Set CH1 VOLTS/cm switch to 20mV, inject 1MHz square wave to give 6cm deflection, adjust trigger to give stable trace.
2. Inspect top of waveform for any step occurring approximately 200μs after the start of the pulse.
3. If any step is present replace A.O.T. resistor, R625, with a small 220Ω carbon potentiometer on short leads, adjust for no step, measure required value and substitute fixed resistors of nearest preferred value.

5.5.14 'ADD MODE' AMPLIFIER BALANCE

1. Set FUNCTION SWITCH to CHOP and bring both traces to the centre horizontal line, by means of CH1 and CH2 SHIFT controls.
2. Set the MODE SWITCH to ADD and note the direction and amount of movement of the trace. Return to CHOP Mode.
3. Add 100kΩ potentiometer across A.O.T. position, R294 or R295, to give a direction of movement the same as that given when moving from CHOP to ADD.
4. Adjust potentiometer to bring both traces to position found in '2'.
5. Re-centre traces, switch to ADD, movement should now be less than 0.5cm.
6. Replace potentiometer with fixed resistor of the nearest preferred value.

5.5.15 CHANNEL 1 and 2 GAIN ADJUSTMENT

1. Set CH1 VOLTS/cm switch to 20mV, INPUT COUPLING switch to dc. FINE GAIN CONTROL to Cal.
2. Inject a 1kHz square wave having an amplitude of 120mV into CH1, adjust R227 (Set Gain CH1) to a deflection of 6cms.
3. Switch to 10mV range, inject 60mV and adjust R138 (CH1) to give 6cm deflection.
4. Switch to 5mV range, inject 30mV and adjust R136 (CH1) to give 6cm deflection.
5. While still on 5mV range, inject 6mV, pull for X5 gain and adjust R229 to give 6cm deflection.
6. Switch to all other ranges and inject the appropriate signal to give 6cm deflection. Check that all ranges are accurate to within ±3%.
7. Repeat the above procedure for Channel 2, the adjustments for the 20mV, 10mV, 5mV and 1mV ranges being respectively, R231, (Set Gain CH2), R138 (CH2) and R136 (CH2). (X5 gain not applicable.)

5.5.16 CHANNEL 1 and 2 ATTENUATOR COMPENSATION

1. Ensure that the attenuator covers are correctly fitted and that the link across the universal coupling on the SHIFT control is continuous.
2. Set CH1 VOLTS/cm switch to 20mV, INPUT COUPLING switch to dc. Inject 200mV 1kHz square wave via the 28pF/1MΩ standardiser. Trigger for stable trace.
3. Adjust input trimmer, C171 (CH1), for square corner.
4. Remove standardiser, switch VOLTS/cm to 0.2V, inject 1V square wave and adjust X10 compensating trimmer, C167 (CH1), for square corner.
5. Inject 2V square wave via standardiser and adjust X10 input trimmer, C165 (CH1), for square corner.
6. Remove standardiser, switch VOLTS/cm to 2V, inject 10V square wave and adjust X100 compensating trimmer, C161 (CH1), for square corner.
7. Inject 20V square wave via standardiser and adjust C100 input trimmer, C159 (CH1), for square corner.
8. Remove standardiser and check all attenuator ranges, applying the appropriate amplitude, to ensure all ranges give a square corner to the applied waveform and are accurate to within ±3%.
9. Repeat above for Channel 2, the component numbering is the same except for a suffix 'CH2'.

5.5.17 Y2 OUTPUT AMPLITUDE AND PHASE ADJUSTMENT

1. Set CH1 and CH2 INPUT VOLTS/cm switches to 0.1V. INPUT COUPLING switches to dc. Link CH2 OUTPUT to CH1 INPUT. FUNCTION SWITCH to ALT. FINE GAIN CONTROL to CAL.
2. Inject 0.5V 1kHz square wave into CH2 input, trigger for a stable trace.
3. Adjust R238 to give equal deflections on CH1 and CH2 (i.e. CH2 Output of 100mV/cm).
4. Remove CH2 OUTPUT link from CH1 INPUT and take to EXT X and PULL X5.
5. Apply a sine wave source to CH1 and CH2. Adjust input level to give a convenient size display which should be a 45° line at low frequencies.
6. With input frequency of 500kHz, adjust capacity (approx. 15pF) C228 (A.O.T.) until ellipse just closes. (Max. phase shift 3°, dc – 500kHz.)

5.5.18 Y AMPLIFIER OVERALL PULSE RESPONSE

1. Set CH1 and CH2 VOLTS/cm switch to 20mV, INPUT COUPLING switch to dc. Ensure that the A.O.T., R230 and R235, are initially not in circuit. FINE GAIN CONTROLS to CAL.
2. Select CH1 mode and inject 100mV square wave at 100kHz. Adjust R309 to give optimum flat top response.
3. Change input frequency to 1MHz. Adjust R311 to give a response having approximately 20% undershoot over the first 35–40ns.
4. Adjust C311 to improve the edge response without affecting adjustment 3.
5. Adjust C322, R357 and C357 for optimum leading edge and corner with no overshoot or hook.
6. Connect a small carbon 1kΩ potentiometer on short leads across A.O.T. pins R230. Adjust potentiometer and C202 to remove undershoot left in adjustment 4 and 5. Replace potentiometer with fixed resistor.
7. Inject 1MHz signal into CH2 and repeat adjustment 6 to establish correct value of R235.
8. Adjust C211 to give improvement in, without increasing, overshoot over first 15μs.

5.5.19 5mV and 10mV HF COMPENSATION

1. Set CH1 and CH2 VOLTS/cm switch to 10mV, INPUT COUPLING switch to dc, FINE GAIN CONTROL to CAL.
2. Select CH1 mode and inject 50mV square wave at 1MHz. Adjust C123 (CH1) to give a square corner.
3. Switch to 5mV/cm, inject 25mV and adjust C122 (CH1) to give a square corner.
4. Repeat 2 and 3 for CH2 input, adjusting C123 (CH2) and C122 (CH1) respectively.

5.5.20 BANDWIDTH

1. Set CH1 and CH2 VOLTS/cm switches to 20mV, INPUT COUPLING switch to dc, FINE GAIN CONTROL to CAL.
2. Select CH1 mode and inject 50kHz from Constant Amplitude Generator to give 5cm deflection. Increase the frequency of the generator until the display amplitude falls to 3.5cms. The frequency should be greater than 40MHz.
3. Repeat '2' for 10mV and 5mV positions on CH1 and for 20, 10 and 5mV positions on CH2.
4. Repeat to 1mV/cm (X5 gain) on CH1 where the bandwidth should be greater than 10MHz.

5.5.21 CHOP WAVEFORM COMPENSATION

1. If any of the transistors or diodes associated with the beam switch are changed it may be necessary to readjust the capacitive balance of the circuit.
2. Set INPUT COUPLING switch to GND. Couple EXT TRIG via probe to the collector of TR218 (R283). Turn TRIG SELECT to EXT.
3. Switch to CHOP mode and set the two traces 0.5cm either side of the centre line by means of the SHIFT controls and adjust the Timebase (1μs/cm) so that individual chop transitions are visible.
4. Small amounts of capacity should be added between points 26 and 25 or 26 and 27 for CH1, and between 29 and 28 or 28 and 30 for CH2, to ensure that the chop transitions are flat and parallel to the centre line. The capacity required is usually small and is most easily achieved by using short lengths of enamelled copper wire twisted together.

TIMEBASE WAVEFORMS

These are drawn for the following conditions. The timebase is switched to 0.1ms/cm and a 5cm 10kHz square wave is applied to the CH1 channel. The trigger is set to CH1 +ve slope.

The video measurements are carried out with a 1V p-p video signal input into 75 ohms, and with the video attenuator set to the 1V range. Normally the instrument is set to display the CLAMP mode, except for the line and field ramp waveforms where PICTURE mode should be selected.

TV ADJUSTMENTS

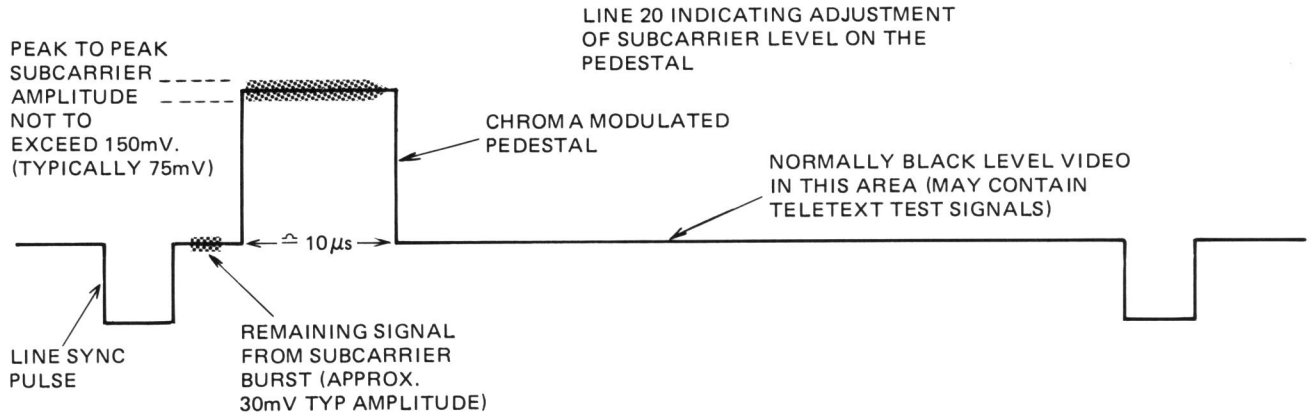
Adjustments to be carried out with the timebase connected on an extension lead, PL91.

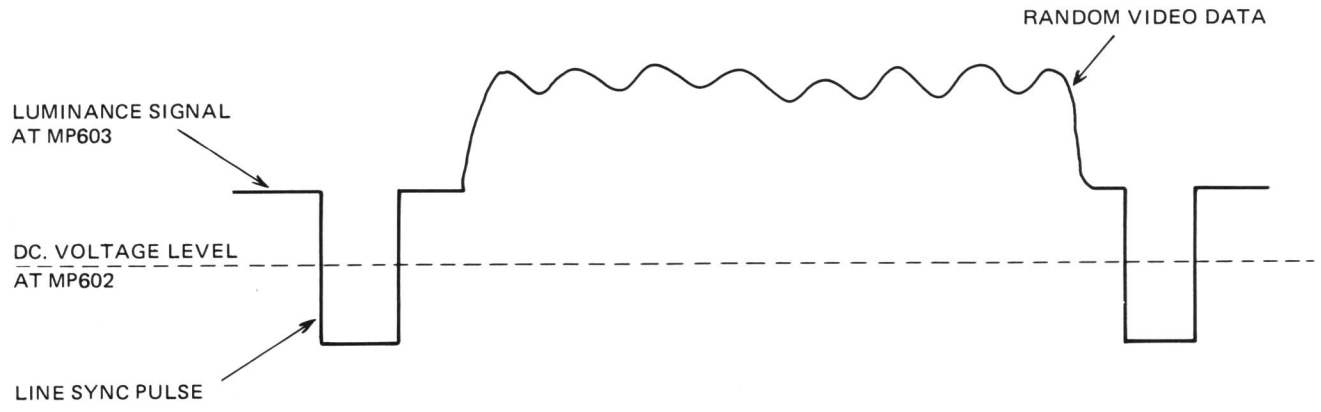
5.5.22 SUBCARRIER TRAP

1. Set the video attenuator to 1V range and the DISPLAY switch to CLAMP OUT. Connect a 1V p-p off-air video source to the video in socket.
2. Connect a X10 probe from the CH2 input on the main frame to TR610 emitter on the monitor point, MP616.
3. Switch the CH2 attenuator to 20mV/cm with input coupling set to ac.
4. Set the LINE SELECT switch to trigger on the line pair 19/332 and observe the chroma modulated pedestal on lines 20/333 (after the staircase). (If TV trigger is not yet functional use a test oscilloscope with TV trigger facilities for this test.)
5. Adjust C614 for minimum 4.43MHz subcarrier on the pedestal. Check that the amplitude is less than 150mV.

5.5.23 SYNC SEPARATOR SLICING LEVEL

1. Set both channels of the test oscilloscope to 20mV and the input switches to dc. Using a X10 probe on each channel input, connect both probes to test point, MP602.
2. Position both traces on the centre horizontal graticule line, then transfer one probe to MP603.
3. Check that the dc signal lies between 45 to 55% of the sync pulse amplitude. If necessary change R674 to achieve this.





5.5.24 DELAY RANGE

1. Connect the VIDEO OUT to the main frame CH2 input. Set the attenuator to 50mV/cm and the input coupling to dc.
2. Set the TRIGGER SELECT switch to TV DELAY (+ve) and the trigger coupling to ac TV. Set the DISPLAY switch to CLAMP OUT.
3. Select the line pair 18/331 on the LINE SELECT switch and check that adjustment of the trigger level control produces a steady triggered video display (not a bright display). Triggering should be stable over approx. 90° of the control range.
4. Check that the DELAY control enables the trigger point to be varied over a range of 90μs ± 10μs.
5. Set the TRIGGER SELECT switch to TV (–ve) and check that a fixed trigger point is obtained before the leading edge of line sync.

5.5.25 LINE SELECT FUNCTIONS

Check that TV trigger functions operate correctly for the following modes. Set the TRIGGER SELECT switch to TV (–ve).

1. EVEN FIELD	trigger point should be just after the first board pulse of Field 1, line 1.
2. ODD FIELDS	trigger point should be just after the first broad pulse on Field 2, line 314.
3. BOTH FIELDS	should produce both the ODD and EVEN Field displays superimposed.
4. LINE REP	triggering occurs on alternate lines and should produce a bright display.
5. LINE SELECTOR	check that the LED display comes on only in this mode. Press the 'UP' push button and check that the count increases slowly for the first four counts and then begins to count more rapidly. Then press the 'DOWN' button and check that the count decreases in a similar manner. Press the 'UP' button and check that the count returns to 1 after the count of 625. Select line 1 and check that trigger occurs just prior to the first board pulse of line 1.
6. LINE PAIRS	a. For UK 625 line system. Select pair 17/330 and check for two teletext lines at the beginning of the display. Select 18/331 and check that only one teletext line is displayed. Select 19/332 and check for triggering just before Pulse, Bar and Staircase (VITS) line. By observing the start of picture video (normally 23/336) check the relative positions of lines 20/333 to 22/335. Also check that 16/329 produces trigger one line before 17/330. b. Other 625 systems Other 625 line PAL systems compatible with this instrument may well have different data preceding the main picture information. In this case a suitable check is best performed by using the LINE SELECTOR to inspect the picture data existing between lines 16 to 22 and comparing this with the information provided by the LINE PAIRS positions on the LINE SELECT switch.

5.5.26 PICTURE

1. Connect the link (PL106) between the rear panel sockets, PICTURE DRIVE and Z MOD.
2. With the off-air signal still connected, switch the DISPLAY SELECT switch to PICTURE.
3. A 625 line picture should now appear on the screen. Set the LINE SELECT switch to the LINE SELECTOR position and set the count display to read about 150.
4. As the DELAY CONTROL is advanced an intensified line should appear about half way down the raster. With the DELAY control set to maximum, the bright line should cover completely one line, starting about 1cm from the end of the line above it and finishing about 1cm after the start of the line below it.
5. Reduce the DELAY control to minimum and the intensified line should reduce to a small dot just before the end of one line. Increase the DELAY to MAX again.
6. Advance the counter by pressing the UP button. Check that the intensified line moves down the raster. Then press the DOWN button and check that the line moves up the screen.

5.5.27 PICTURE SIZE

1. Check that the picture height is 6.5cms (±10%), 6cms of main picture + about 0.5cm of pre-picture data.
2. The picture width should be 8cms (±10%). If not adjust the value of R759 (A.O.T.) to achieve this.

5.5.28 SUBCARRIER TRAP

1. Switch the DISPLAY switch to CLAMP.
2. Connect a X10 probe from the test oscilloscope to monitor point MP605. Adjust C606 for minimum colour burst during the back porch clamp pulse period. If C606 has insufficient range change the A.O.T. component, C607, to 330pF or 390pF.

5.5.29 DC LEVEL

1. Disconnect the video input signal.
2. Connect the digital multimeter on a 100mV range

to MP604. Set the potentiometer, R617, for 0V ±5mV.

3. Connect the VIDEO OUT to CH2 input. Set the CH2 input to GND and the attenuator to 10mV/cm. Then centre the trace on the crt.
4. With the DISPLAY switch still in the CLAMP position check that not more than ±20mV of offset between GND and dc input coupling positions. If necessary change the value of R625 (A.O.T.) to achieve this.
5. Now adjust R617 for no movement on the trace when the CH2 input is switched between GND and dc (within ±5mV).
6. With the trace centred on the middle line of the graticule and the input of CH2 set to dc, connect the off-air video signal to the VIDEO IN socket. Black level occurring during the Back Porch should be maintained at 0V ±5mV.

5.5.30 CALIBRATOR ADJUSTMENT

1. Disconnect the leads connecting to the VIDEO IN and VIDEO OUT sockets. Now connect a digital multimeter on the 1V range across the centre pin and chassis earth of the VIDEO OUT socket.
2. Now it is necessary to stop the calibrator oscillating by connecting a shorting link between TR644 emitter and chassis earth. (This is conveniently done by connecting to the appropriate end of R783 and the timebase main chassis.)
3. With the 'CAL' front panel button pressed adjust the potentiometer, R786, for 250.0mV on the DMM, and then release the button.
4. Now reconnect the DMM input to the 1V calibrator output pin on the front panel. Check that this reads 1V ±1%. The shorting link on TR644 emitter should now be removed.
5. Reconnect the off-air signal to the VIDEO IN and the link from VIDEO OUT to CH2. Set CH2 to 50mV/cm and dc coupling. Set the timebase range to 1ms/cm and the trigger to CH2 +ve and AUTO-level.
6. When the CAL push button is pressed the video signal should be interrupted and a 5cm square wave signal (±3%) should appear on the crt. Then adjust the calibrator frequency by R781 so that 1 cycle/cm appears against the graticule markings. (The calibrator frequency should be 1kHz ±5%.)

5.5.31 INPUT IMPEDANCE

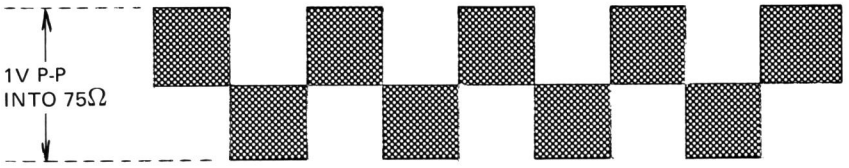
1. Disconnect the off-air video signal from the VIDEO IN socket and connect the digital multimeter on the 100Ω range between the centre pin of the socket and chassis ground.
2. Check that the input impedance is maintained at 75Ω ±1% over all three ranges of the attenuator 0.5V, 1V and 2V.

VIDEO ATTENUATOR CALIBRATION

1. Switch the DISPLAY switch to CLAMP OUT and remove the link connecting the VIDEO OUT to CH2 input.
2. Connect a dc supply source of voltage set to about 1V to the VIDEO IN socket centre pin and the 0V to chassis earth.
3. Connect the DMM on the 1V range across the VIDEO OUT socket. Set the video attenuator on the 1V range and adjust the dc supply for a reading of 250.0mV on the DMM.
4. Now switch to the 2V video attenuator range and check that the reading is 125mV ±0.5%.
5. Finally switch to the 0.5V range and check for a DMM reading of 500mV ±0.5%.

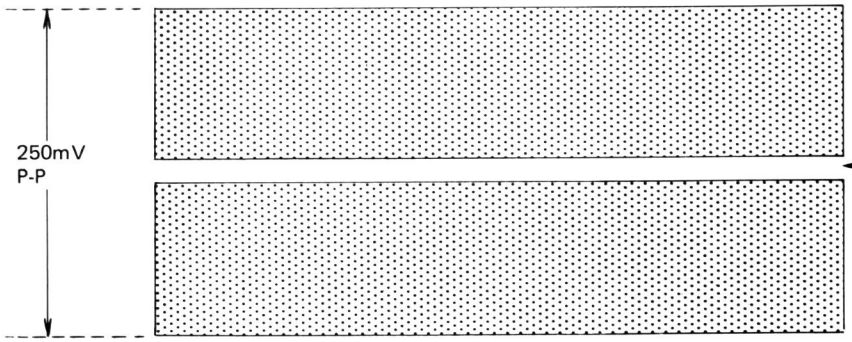
5.5.32 CLAMP OUT CALIBRATION

1. Connect the VIDEO OUT to CH2 input link. The DISPLAY switch should be set to CLAMP OUT.
2. Set CH2 input to dc 20mV/cm. The timebase range switch should be set to 0.5ms/cm and the trigger to CH2 +ve with AUTO level.
3. Press the CAL button and adjust the CH2 variable gain control for exactly 8cms display. This control setting should now be left for the next stage.
4. Connect the 10kHz 1V square wave output from the colour calibrator to the VIDEO IN socket. With the video attenuator on the 1V range check for 8cms vertical deflection on the crt to be within ±1% (±0.8mm).
5. Now switch the colour calibrator to give 10kHz + 4.43MHz output (500mV @ 10kHz, +500mV @ 4.43MHz). Set CH2 attenuator to 20mV/cm with the variable gain to the CAL position. Set the TRIGGER SELECT to the FREE RUN position.
6. The 10kHz modulated subcarrier will produce a continuous untriggered display on the screen. By observing the mid point of the signal and operating the ±0.1dB switch (which adjusts the amplitude of the subcarrier) check that the subcarrier is made to overlap or open out by equal amounts. If the movement of the subcarrier is not symmetrical adjust A.O.T., C611, on the video attenuator until this condition can be achieved.



4.4MHz SUBCARRIER MODULATED BY 10kHz SQUARE WAVE.

OUTPUT FROM COLOUR CALIBRATOR.



THE SAME SIGNAL VIEWED AT THE OUTPUT FROM VIDEO OUT SOCKET WITH TIMEBASE ON FREE RUN.

ALIGN C611 TO GIVE EQUAL GAP/OVERLAP OF SUBCARRIER BY ADJUSTMENT OF ±0.1dB SWITCH. AT CAL POSITION SUBCARRIER TRACES SHOULD JUST MERGE.

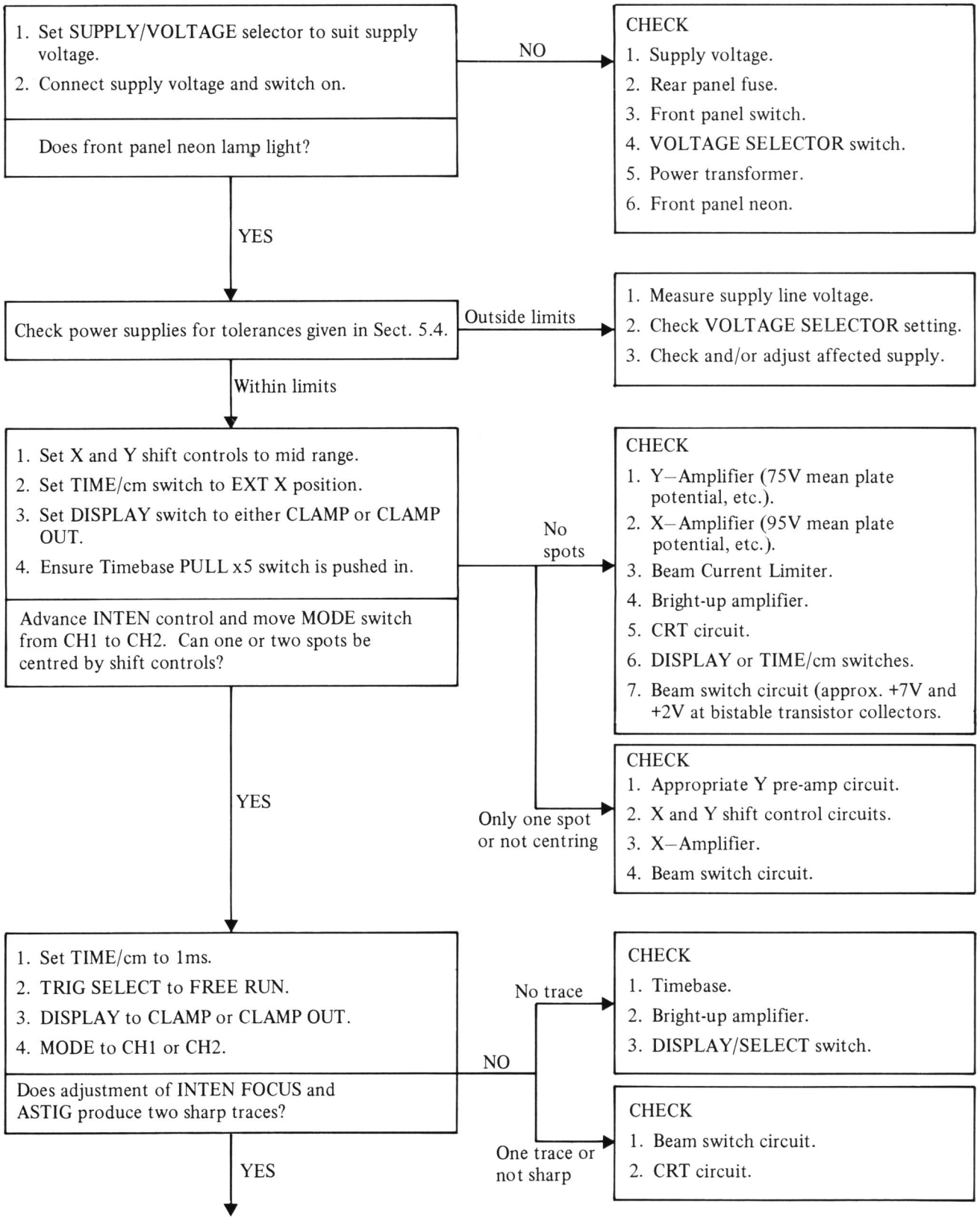
5.5.33 CLAMP GAIN CALIBRATION

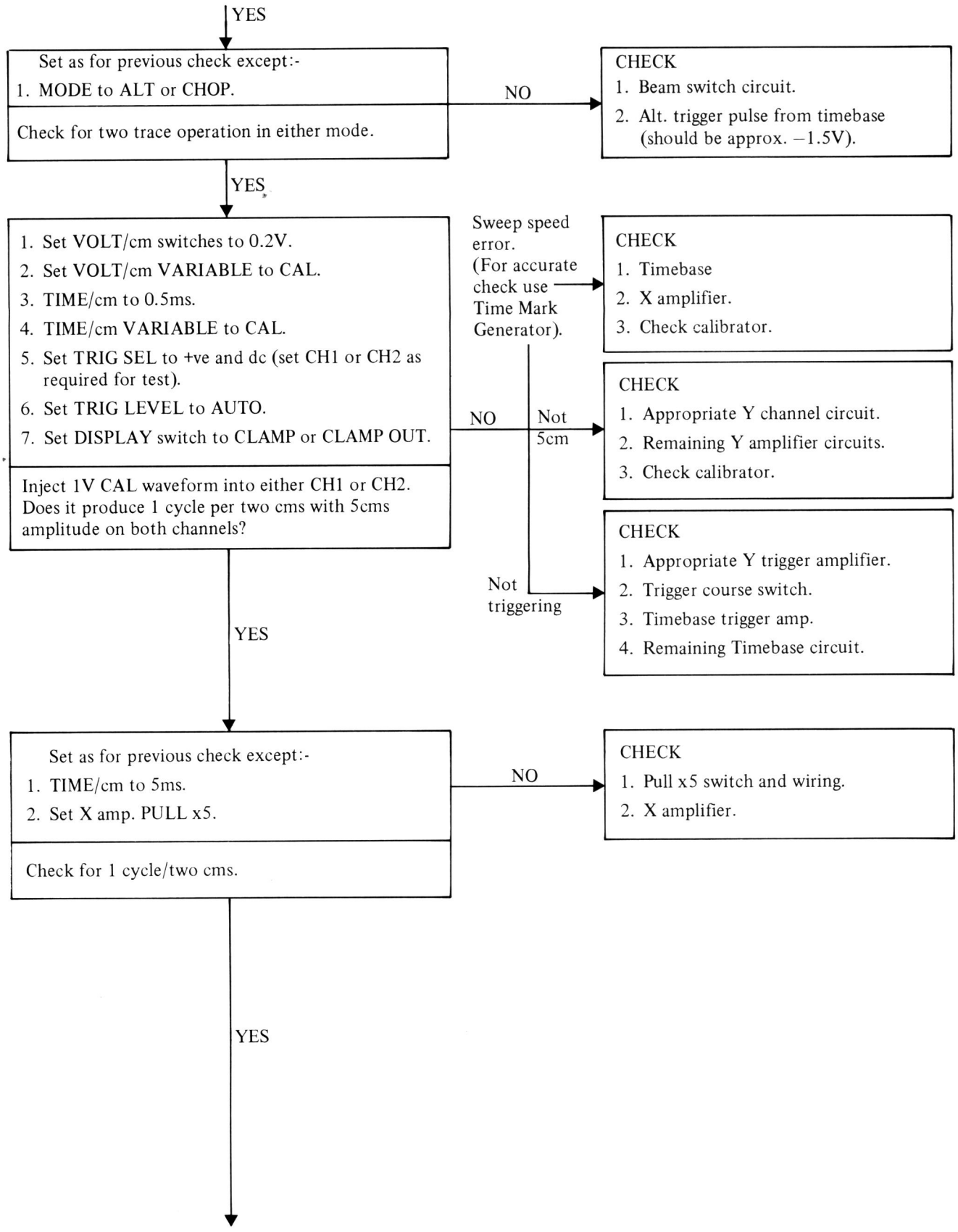
1. Set the DISPLAY switch to CLAMP. CH2 input to 20mV/cm. Set the TRIGGER SELECT switch to CH2 +ve and trigger to AUTO.
2. Remove IC600 (CD4098) from its socket to disable the clamp.
   NB. It is preferable to switch the instrument off while performing this operation to avoid damage to the circuitry.
3. Press the CAL button and adjust the variable CH2 gain control for exactly 8cms display. With the video attenuator set to the 1V position connect the 1V @ 10kHz input from the colour calibrator and check that the display amplitude is 8cms within less than ±1%. If necessary select a value for R628 which gives the closest match to 8cms.

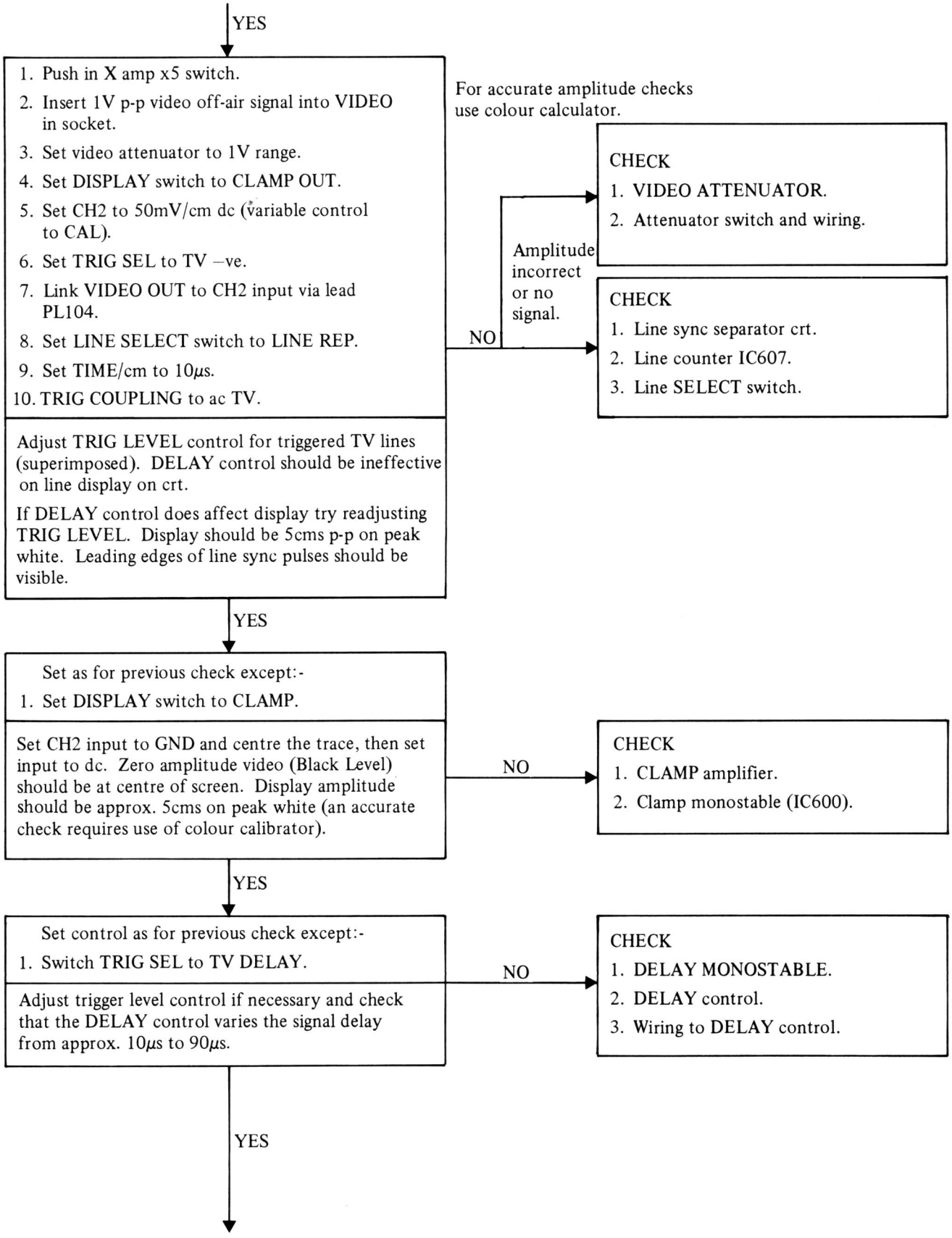
(Note: IC600 must be removed to disable clamp and prevent distortion on high negative signal amplitude.)

4. Replace IC600.
5. Switch the DISPLAY switch to CLAMP OUT and check for agreement of 8cms display amplitude within ±1% of the CLAMP amplitude. If not re-select the value of R628 to achieve this limit and that of stage 3.
6. Switch the DISPLAY switch to CLAMP. Set the colour calibrator to give a 500mV modulated 10kHz + subcarrier and adjust C605 (A.O.T.) to give equal overlap of subcarrier by a similar manner to that employed in the CLAMP OUT calibration previously described (stages 5 and 6).

FAULT LOCALISATION CHART




YES
Set as for previous check except:-
1. MODE to ALT or CHOP.
Check for two trace operation in either mode.
NO
CHECK
1. Beam switch circuit.
2. Alt. trigger pulse from timebase (should be approx. −1.5V).
YES
1. Set VOLT/cm switches to 0.2V.
2. Set VOLT/cm VARIABLE to CAL.
3. TIME/cm to 0.5ms.
4. TIME/cm VARIABLE to CAL.
5. Set TRIG SEL to +ve and dc (set CH1 or CH2 as required for test).
6. Set TRIG LEVEL to AUTO.
7. Set DISPLAY switch to CLAMP or CLAMP OUT.
Inject 1V CAL waveform into either CH1 or CH2. Does it produce 1 cycle per two cms with 5cms amplitude on both channels?
Sweep speed error. (For accurate check use Time Mark Generator).
CHECK
1. Timebase
2. X amplifier.
3. Check calibrator.
NO
Not 5cm
CHECK
1. Appropriate Y channel circuit.
2. Remaining Y amplifier circuits.
3. Check calibrator.
Not triggering
CHECK
1. Appropriate Y trigger amplifier.
2. Trigger course switch.
3. Timebase trigger amp.
4. Remaining Timebase circuit.
YES
Set as for previous check except:-
1. TIME/cm to 5ms.
2. Set X amp. PULL x5.
Check for 1 cycle/two cms.
NO
CHECK
1. Pull x5 switch and wiring.
2. X amplifier.
YES


YES
1. Push in X amp x5 switch.
2. Insert 1V p-p video off-air signal into VIDEO in socket.
3. Set video attenuator to 1V range.
4. Set DISPLAY switch to CLAMP OUT.
5. Set CH2 to 50mV/cm dc (variable control to CAL).
6. Set TRIG SEL to TV –ve.
7. Link VIDEO OUT to CH2 input via lead PL104.
8. Set LINE SELECT switch to LINE REP.
9. Set TIME/cm to 10μs.
10. TRIG COUPLING to ac TV.
For accurate amplitude checks use colour calculator.
CHECK
1. VIDEO ATTENUATOR.
2. Attenuator switch and wiring.
Amplitude incorrect or no signal.
NO
CHECK
1. Line sync separator crt.
2. Line counter IC607.
3. Line SELECT switch.
Adjust TRIG LEVEL control for triggered TV lines (superimposed). DELAY control should be ineffective on line display on crt.
If DELAY control does affect display try readjusting TRIG LEVEL. Display should be 5cms p-p on peak white. Leading edges of line sync pulses should be visible.
YES
Set as for previous check except:-
1. Set DISPLAY switch to CLAMP.
Set CH2 input to GND and centre the trace, then set input to dc. Zero amplitude video (Black Level) should be at centre of screen. Display amplitude should be approx. 5cms on peak white (an accurate check requires use of colour calibrator).
NO
CHECK
1. CLAMP amplifier.
2. Clamp monostable (IC600).
YES
Set control as for previous check except:-
1. Switch TRIG SEL to TV DELAY.
Adjust trigger level control if necessary and check that the DELAY control varies the signal delay from approx. 10μs to 90μs.
NO
CHECK
1. DELAY MONOSTABLE.
2. DELAY control.
3. Wiring to DELAY control.
YES

YES

Set controls as for previous check except:-

1. Switch to PICTURE display.
2. Link VIDEO DRIVE to Z MOD input on rear panel of instrument.

Initially set DELAY control to minimum and check that a raster of approx. 6cms x 8cms appears on crt. Then advance DELAY control and check that the picture brightness is intensified, progressively towards the right of the picture. With DELAY at max. the entire raster should be intensified.

NO

No picture
No scan → CHECK
1. Video Drive amp.
2. Z mod amp.
3. Video link.
4. +24V supply to Line and Field scan circuits.
5. S601.

Vertical scan but no horizontal scan → CHECK
1. Line Ramp Generator.
2. Display Switch S601.
3. X Gate to X amplifier.

Horizontal but no vertical scan → CHECK
1. Field Ramp Generator.
2. Field Pulse separator.
3. Display Switch S601.

YES

Raster but no modulation → CHECK
1. Video Drive amp.
2. Z mod amp.
3. Video link.
4. Wiring to Video Drive amp.
5. Display switch S601.

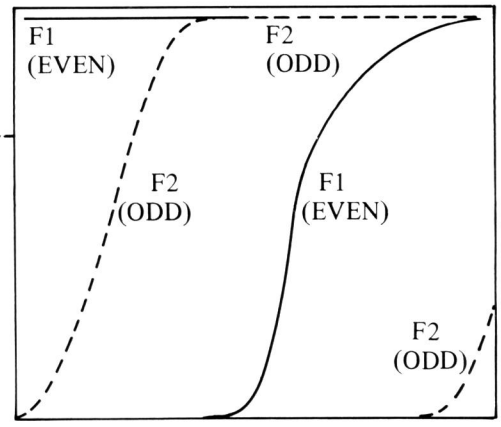
Full picture with modulation but no bright-up from delay control → CHECK
1. Delay Monostable.
2. Transistor TR635 and associated components in video drive amp.

Set controls as for previous check except:-

1. Set DELAY to max.

Initially set LINE SELECT to EVEN Fields, then set to ODD Fields, and finally to BOTH Fields. Check that the bright-up display is as per the inset diagram for each field and then for both fields together.

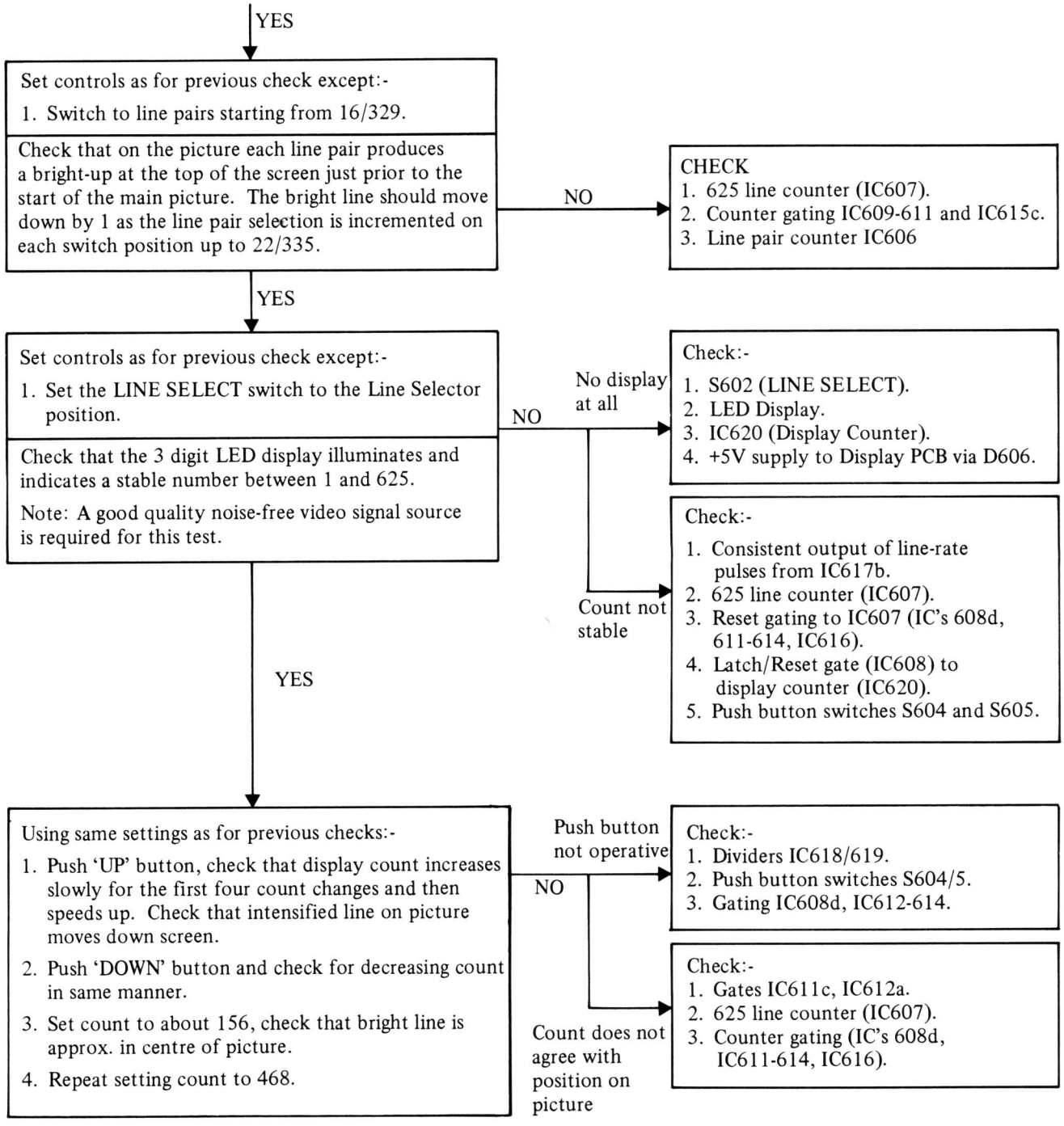
DISPLAYED PICTURE



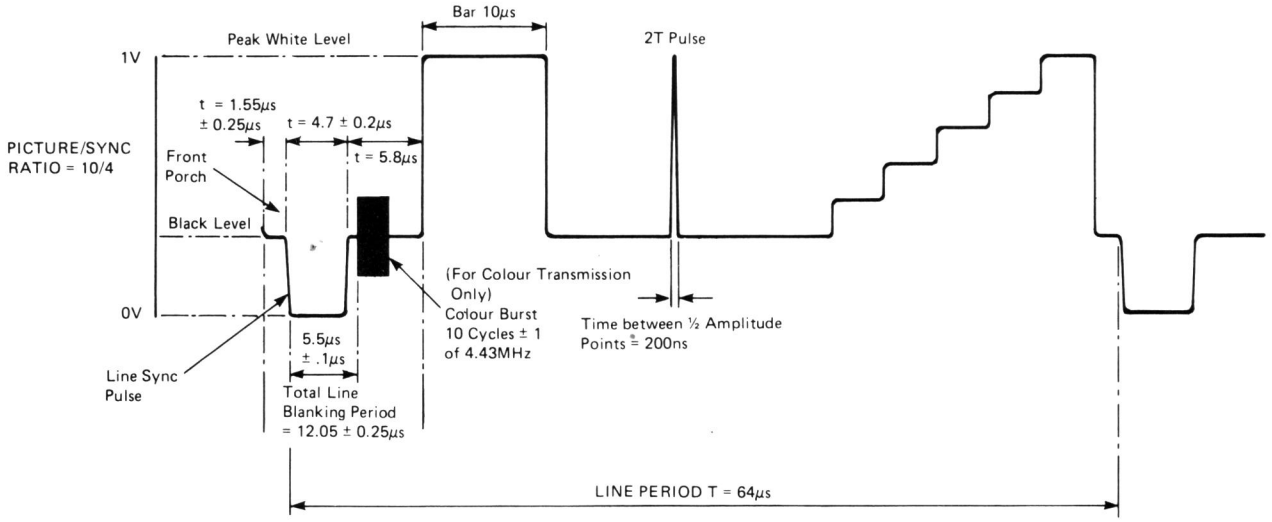
NO

CHECK
1. Field sync discriminator (IC605).
2. S602 + wiring.

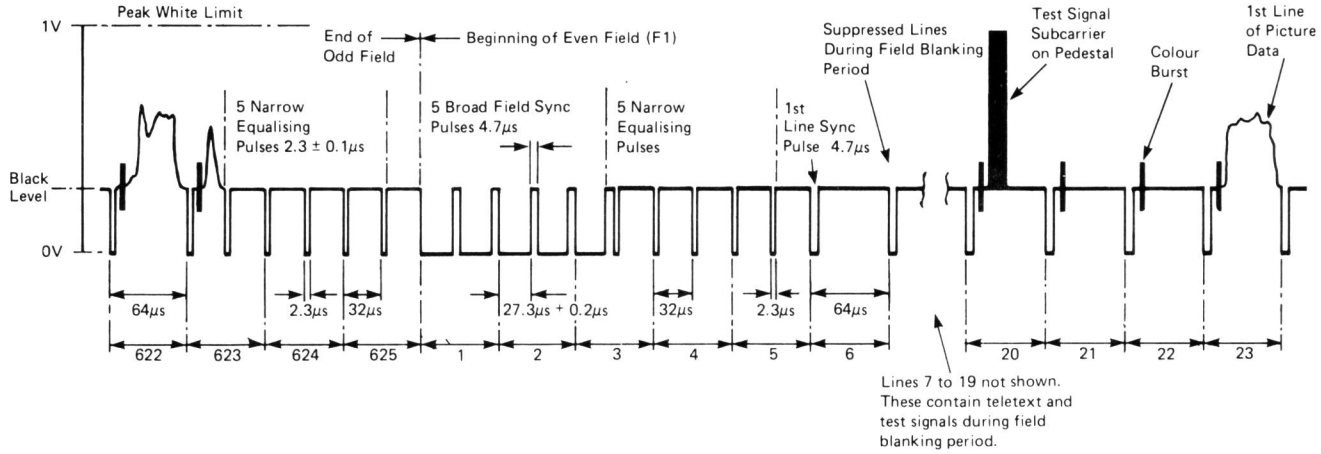
YES


YES
Set controls as for previous check except:-
1. Switch to line pairs starting from 16/329.
Check that on the picture each line pair produces a bright-up at the top of the screen just prior to the start of the main picture. The bright line should move down by 1 as the line pair selection is incremented on each switch position up to 22/335.
NO
CHECK
1. 625 line counter (IC607).
2. Counter gating IC609-611 and IC615c.
3. Line pair counter IC606
YES
Set controls as for previous check except:-
1. Set the LINE SELECT switch to the Line Selector position.
Check that the 3 digit LED display illuminates and indicates a stable number between 1 and 625.
Note: A good quality noise-free video signal source is required for this test.
NO
No display at all
Check:-
1. S602 (LINE SELECT).
2. LED Display.
3. IC620 (Display Counter).
4. +5V supply to Display PCB via D606.
Count not stable
Check:-
1. Consistent output of line-rate pulses from IC617b.
2. 625 line counter (IC607).
3. Reset gating to IC607 (IC's 608d, 611-614, IC616).
4. Latch/Reset gate (IC608) to display counter (IC620).
5. Push button switches S604 and S605.
YES
Using same settings as for previous checks:-
1. Push 'UP' button, check that display count increases slowly for the first four count changes and then speeds up. Check that intensified line on picture moves down screen.
2. Push 'DOWN' button and check for decreasing count in same manner.
3. Set count to about 156, check that bright line is approx. in centre of picture.
4. Repeat setting count to 468.
Push button not operative
NO
Check:-
1. Dividers IC618/619.
2. Push button switches S604/5.
3. Gating IC608d, IC612-614.
Count does not agree with position on picture
Check:-
1. Gates IC611c, IC612a.
2. 625 line counter (IC607).
3. Counter gating (IC's 608d, IC611-614, IC616).

1. SINGLE LINE OF VIDEO: PICTURE DATA INCLUDES A 10μs BAR, 2T PULSE & STAIRCASE (TYPICAL TEST WAVEFORM)



2. FIELD WAVEFORMS: a) EVEN (F1) FIELD



b) ODD (F2) FIELD

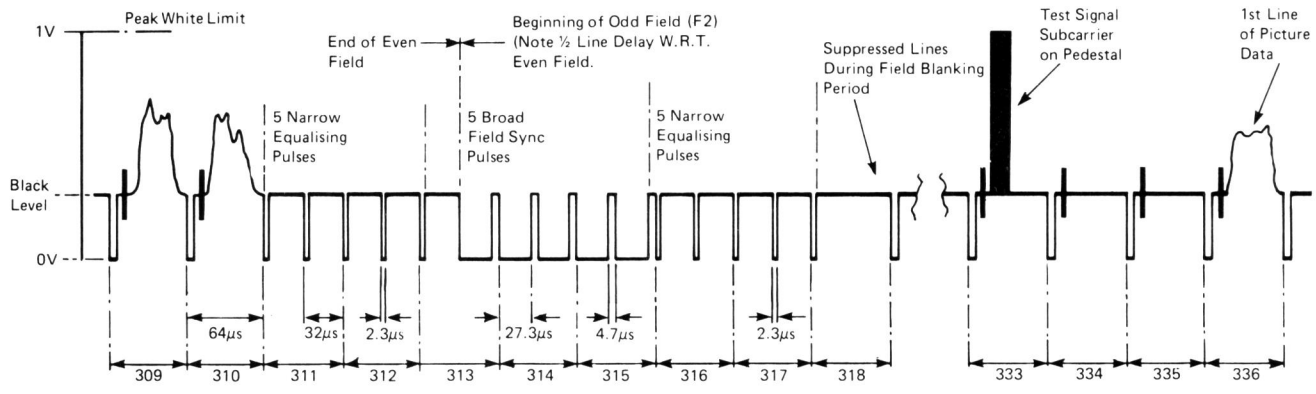


Fig. 2 625 line TV Waveforms

Component List and Illustrations

Section 6

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

RESISTORS

CC	Carbon Composition	½ W	10%	unless otherwise stated
CF	Carbon Film	⅛ W	5%	unless otherwise stated
MO	Metal Oxide	½ W	2%	unless otherwise stated
MF	Metal Film	¼ W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potentiometer Type MPD, PC		20%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+ 80% − 25%	
CE(2)	Ceramic	500V	± 10%	unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		± 10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		± 10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (Aluminium)		+ 50% − 10%	
T	Tantalum		+ 50% − 10%	

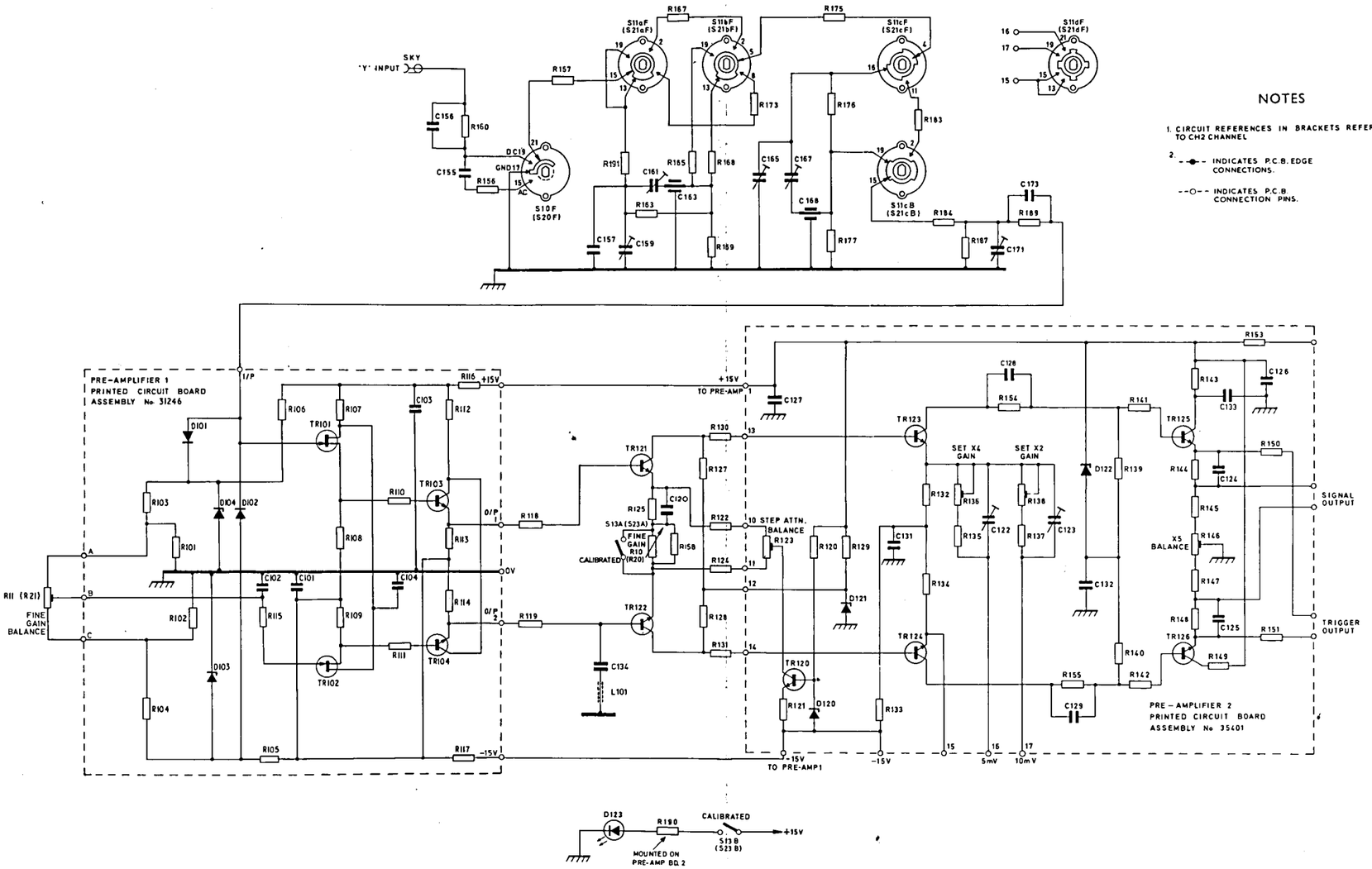
OS3300A PRE-AMP 1 & 2 AND GAIN SWITCHING

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R10	470	CP	With S13	34779
R11	500	CP		A4/31250
R101	270	CF		28720
R102	270	CF		28720
R103	3k3	CF		21803
R104	3k3	CF		21803
R105	1k2	CF		21800
R106	1k2	CF		21800
R107	1k	CF		21799
R108	4k7	CF		21805
R109	4k7	CF		21805
R110	47	CF		28714
R111	47	CF		28714
R112	680	CF		28723
R113	3k3	CF		21803
R114	3k3	CF		21803
R115	100	CF		21794
R116	10	CF		21793
R117	10	CF		21793
R118	56	CF		28715
R119	10	CF		21793
R120	3k9	CF		21804
R121	680	CF		28723
R122	1k	CF		21799
R123	100	CP		33700
R124	1k	CF		21799
R125	110	MO		28783
R126	Not Used			
R127	330	MO		26741
R128	330	MO		26741
R129	560	CF		21798
R130	10	CF		21793
R131	47	CF		28714
R132	390	MO		26740
R133	1k5	CF		21801
R134	390	MO		26740
R135	180	CF		21795
R136	100	Erie Type 81		36254
R137	680	CF		28723
R138	220	PCP		36253
R139	100	MO		26747
R140	100	MO		26747
R141	10	CF		21793
R142	10	CF		21793
R143	100	CF		21794
R144	100	CF		21794
R145	2k2	CF		21802
R146	1k	PCP		36256
R147	2k2	CF		21802
R148	100	CF		21794
R149	100	CF		21794
R150	270	CF		28720
R151	270	CF		28720
R152				
R153	10	CF		21793
R154	390	MO		26740
R155	390	MO		26740
R156	10	CF		21793
R157	10	CF		21793
R158	820	CF		28724
R159				
R160	27	CF		28711
R163	990k	MF		31927
R164				
R165	39	CF		28713
R166				
R167	10	CF		21793
R168	47	CF		28714
R169	10k1	MF		31928
R173	27	CF		28711
R174				
R175	10	CF		21793
R176	900k	MF	5	31929
R177	111k	MF	5	31930
R183	10	CF		21793
R184	10	CF		21793
R187	1M	MF	5	26346
R188				
R189	330k	CC		4408
R190	1k	CF		21799
R191	22Ω	CC	$\frac{1}{8}$W	28710
CAPACITORS				
C101	.01μF	CE(2)		22395
C102	.01μF	CE(2)		22395
C103	.01μF	CE(2)		22395
C104	.01μF	CE(2)		22395
C120	4.7pF	CE(2)		4502
C121		E		
C122	3/13pF	TRIMMER		32059
C123	.7/6pF	TRIMMER		29421
C124	220pF	CE(2)		22379
C125	220pF	CE(2)		22379
C126	.01μF	CE(2)		22395
C127	.01μF	CE(2)		22395
C128	.01μF	CE(2)		22395
C129	.01μF	CE(2)		22395
C130				
C131	.01μF	CE(2)		22395
C132	.01μF	CE(2)		22395
C133	.01μF	CE(2)		22395
C134	8.2pF	CE(2)		22363
C155	.1μF	CE(2)	400V	29495

OS3300A PRE-AMP 1 & 2 AND GAIN SWITCHING (Contd.)

Ref	Value	Description	Tol % ±	Part No
CAPACITORS (Cont.)				
C156	47pF	CE(2)		22372
C157	10pF	CE(2)		4504
C158				
C159	.7/6pF	TRIMMER		25750
C160				
C161	.7/6pF	TRIMMER		25750
C162				
C163	330pF	CE(2)		31293
C164				
C165	.7/6pF	TRIMMER		25750
C166				
C167	.7/6pF	TRIMMER		25750
C168	47pF	CE(2)		29918
C171	.5/3pF	TRIMMER		42056
C172				
C173	5600pF	CE(2)		22394
TRANSISTORS				
TR101, TR102		AE12	Matched Pair	A31253
TR103, TR104		AE13	Matched Pair	A31254
TR120		2N2369		23307
TR121, TR122		AE13	Matched Pair	A31254
TR123		FTR129		40315
TR124		FTR129		40315
TR125		FTR129		40315
TR126		FTR129		40315
DIODES				
D101		FD300		35592
D102		FD300		35592
D103	6V2	ZENER		33930
D104	6V2	ZENER		33930
D120	7V5	ZENER		22173
D121	5V6	ZENER		33929
D122	5V1	ZENER		20218
D123	209A	L.E.D. T.I.L.		35202
MISCELLANEOUS				
L101				26986
S10				A2/31292
S11				35470
S12				
S13			With R10	34779
SKY				1222

RESISTORS	R11 (R21) R103 R101 R102 R104 R106 R105 R115 R107 R108 R109 R110 R111 R116 R160 R112 R113 R156 R114 R118 R119 R157 R191 R163 R125 R10 R190 R167 R158 R127 R128 R165 R164 R169 R130 R122 R124 R131 R173 R123 R121 R120 R175 R176 R177 R129 R183 R133 R132 R134 R184 R187 R136 R135 R189 R154 R138 R137 R155 R139 R140 R141 R142 R143—R149 R153 R150 R151
CAPACITORS	C102 C101 C103 C104 C156 C155 C134 C157 C120 C159 C161 C163 C165 C127 C167 C168 C131 C171 C128 C122 C173 C123 C129 C132 C133 C124 C125 C126
MISC.	D101 D104 D102 D103 TR101 TR102 SKY TR103 TR104 S10F (S20F) L101 D123 S11aF (S21aF) TR121 TR122 S13A (S23A) S11bF (S21bF) S13B (S23B) TR120 D120 D121 S11cF (S21cF) S11cB (S21cB) TR123 TR124 S11dF (S21dF) D122 TR125 TR126



NOTES

1. CIRCUIT REFERENCES IN BRACKETS REFER TO CH2 CHANNEL
2. --●-- INDICATES P.C.B. EDGE CONNECTIONS.
   --○-- INDICATES P.C.B. CONNECTION PINS.

Fig. 2 Circuit Diagram Pre-amp 1 & 2 and Gain Switching

OS3350 DELAY LINE DRIVER & BEAM SWITCH

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R200	10	CF		21793
R201	10	CF		21793
R202	10	CF		21793
R203	270	MO		26742
R204	10	CF		21793
R205	10	CF		21793
R206	270	MO		26742
R207	10	CF		21793
R208	10	CF		21793
R209	10	CF		21793
R210	10	CF		21793
R211	10	CF		21793
R212	56	CF		28715
R213	100	PCP		28520
R214	220	MO		26743
R215	1k5	CF		21801
R216	330	MO		26741
R217	180	CF		21795
R218	330	MO		26741
R219	330	MO		26741
R220				
R221	330	MO		26741
R222	56	CF		28715
R223	100	PCP		28520
R224	220	MO		26743
R225	1k5	CF		21801
R226	680	CF		28723
R227	2k2	PCP		24561
R228	68	CF		28716
R229	100	PCP		28520
R230	100	CF A.O.T.		21794
R231	2k2	PCP		24561
R232	680	CF		28723
R233	100	PCP		28520
R234	68	CF		28716
R235	100	CF A.O.T.		21794
R236	68	CF		28716
R237	470	CF		21797
R238	470	PCP		28524
R239	39k	CF		28278
R240	1k8	CF		28725
R241	56	CF		28715
R242	2k2	CF		21802
R243	15k	CF		28727
R244				
R245	3k9	MO		26724
R246	3k9	MO		26724
R247	470	MO		26739
R248	470	MO		26739
R249	330	MO		26741
R250	330	MO		26741
R252				
R252	820	MO		26736
R253	820	MO		26736
R254	22	CF		28710
R255	1k8	CF		28725
R256	22	CF		28710
R257	1k2	MO		26734
R258	10	CF		21793
R259	10	CF		21793
R260	47	CF		28714
R261	120	CF		28718
R262	390	MO		26740
R263	39	CF		28713
R264	39	CF		28713
R265	180	CF A.O.T.		21795
R266	56	CF		28715
R267	150	CF		28719
R268	1k	CF		21799
R269	4k7	CF		21805
R270	820	CF		28724
R271	3k9	CF		21804
R272	3k9	CF		21804
R273	820	CF		28724
R274	10	CF		21793
R275	10	CF		21793
R276	4k7	CF		21805
R277	1k	CF		21799
R278	150	CF		28719
R279	390	CF		28722
R280	10k	CF		21809
R281	2k2	CF		21802
R282	3k3	CF		21803
R283	3k9	CF		21804
R284	1k8	CF		28725
R285	2k4	MO		26729
R286	470	CF		21797
R287	2k7	CF		28726
R288	10	CF		21793
R289	10	CF		21793
R290	10	CF		21793
R291	47	CF		28714
R292	47	CF		28714
R293				
R294		A.O.T.		
R295		A.O.T.		
R296	100	CF		21794
CAPACITORS				
C200	100pF	CE(2)		22376
C201	.01μF	CE(2)		22395
C202	3.5/13pF	TRIMMER		18803
C203	.1μF	CE(1)	30V	19647
C204	100pF	CE(2)		22376
C205	.1μF	CE(1)	30V	19647
C206	3.5/13pF	TRIMMER		18803
C209	15pF	CE(2)		22366
C210	15pF	CE(2)		22366
C211	10/40pF	TRIMMER		29483

OS3350 DELAY LINE DRIVER & BEAM SWITCH (Contd.)

Ref	Value	Description	Tol % ±	Part No
CAPACITORS (Cont.)				
C212	470pF	CE(2)		22383
C213	33pF	CE(2)		22370
C214	.01μF	CE(2)		22395
C215	22pF	CE(2)		22368
C216	22pF	CE(2)		22368
C217	.01μF	CE(2)		22395
C218	33pF	CE(2)		22370
C219	470pF	CE(2)		22383
C220	.01μF	CE(2)		22395
C221	900pF		1 125V	24885
C222	.01μF	CE(2)		22395
C223	47pF	CE(2)		22372
C224	.01μF	CE(2)		22395
C225	.1μF	CE(1)	30V	19647
C226	22μF	E	25V	32181
C227	3300pF	CE(2)		22391
C228	15pF	CE(2) A.O.T.		22366
C229	3300pF	CE(2)		22391
C230	150pF	CE(2)		22378
C231	150pF	CE(2)		22378
C232	100μF	E	25V	32183
TRANSISTORS				
TR201		AE16		A31781
TR202		AE16		A31781
TR203		AE16		A31781
TR204		AE16		A31781
TR205 } TR206 }		AE17 Matched Pair		A32063
TR207		AE16		A31781
TR208		AE16		A31781
TR209		2N2369 I.T.T. Only		33701
TR210		2N2369 I.T.T. Only		33701
TR211		2N2369 I.T.T. Only		33701
TR212		AE16		A31781
TR213		AE16		A31781
TR214		AE16		A31781
TR215		2N2369 I.T.T. Only		33701
TR216		2N2369 I.T.T. Only		33701
TR217		2N2369 I.T.T. Only		33701
TR218		2N2369 I.T.T. Only		33701
DIODES				
D201		1N916		1949
D202		1N916		1949
D203		1N916		1949
D204		1N916		1949
D205		1N916		1949
D206		1N916		1949
D207		1N916		1949
D208		1N916		1949
D209	5V6	ZENER		33929
D210				
D211		1N4148		23802
D212		1N4148		23802

| | | |

OS3350 DELAY EQUALISER & OUTPUT DRIVER

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R300	1k8	CF	A.O.T.	28725
R301	100	MO		26747
R302	100	MO		26747
R303	3k3	CF		21803
R304	22	CF		28710
R305	22	CF		28710
R306	390	MO		26740
R307	390	MO		26740
R308	12k	CF		21810
R309	22k	PCP		25885
R310	15k	CF		28727
R311	10k	PCP		28525
R312	390	MO		26740
R313	39	CF		28713
R314	39	CF		28713
R315	100	CF		21794
R316	100	CF		21794
R317	560	MO		36737
R318	100	MO		26747
R319	100	MO		26747
R320	47	CF		28714
R321	22	CF		28710
R322	22	CF		28710
R323				
R324	2k2	PCP		24561
R325	3k3	CF		21803
R326	3k3	CF		21803
R327	56	MO		28777
R328	56	MO		28777
R329	560	MO		26737
R330	150	MO		26745
R331	150	MO		26745
R335	10	CF		21793
R336	10	CF		21793
R337				
R338	100k	CF		21819
R339	220	PCP		36262
R350	10	CF		21793
R351	2k2	CF		21802
R352	47	CF		28714
R353	51	MF	2W	38563
R354	56	MO		28777
R355	56	MO		28777
R356	10	CF		21793
R357	100	PCP		28520
R358	270	CF		28720
R359	10	CF		21793
R360	56	MO		28777
R361	56	MO		28777
R362	56	CF		28715
R363	56	CF		28715
R364	56	CF		28715
R365	680	MO	5 2W	40452
R366	270	CF		28720
R367	3k3	CF		21803
R368	680	MO	5 2W	40452
R369				
R370	680	MO	5 2W	40452
R371	680	MO	5 2W	40452
R372	3k3	CF		21803
R373	270	CF		28720
R374	10	CF		21793
R375	100	CF		21794
R376	1k8	CF		28725
R377	10	CF		21793
R378	270	CF		28720
R379	680	CF		28723
R380				
R381	220k	PCP		29363
R382	120k	CF		21820
R383	1k5	WW		598
R384	100	CF		21794
R385	10	CF		21793
R386	150	CF		28719
R387	2.2k	MO		26730
CAPACITORS				
C301	1000pF	CE(2)		22387
C302	.22μF	PE	160V	31379
C303	82pF	CE(2)		22375
C304	1000pF	CE(2)		22387
C305	1000pF	CE(2)		22387
C306	47pF	CE(2)		22372
C307	.01μF	CE(2)	250V	22395
C308	.01μF	CE(2)	250V	22395
C309	.01μF	CE(2)	250V	22395
C310				
C311	10/40pF	TRIMMER		29483
C312	27pF	CE(2)		22369
C313	33μF	E	16V	32173
C314	33μF	E	16V	32173
C315	1000pF	CE(2)		22387
C316	1000pF	CE(2)		22387
C317	.01μF	CE(2)	250V	22395
C318	.01μF	CE(2)	250V	22395
C321	4.7pF	CE(2)		4502
C322	3.5/13pF	TRIMMER		18803
C351	27pF	CE(2)		22369
C352	100pF	CE(2)		22376
C353	100pF	CE(2)		22376
C354	.01μF	CE(2)	250V	22395
C355	.01μF	CE(2)	250V	22395
C356	.01μF	CE(2)	250V	22395
C357	10/60pF	TRIMMER		37347
C358	.01μF	CE(2)	250V	22395
C359	.01μF	CE(2)	250V	22395
C360	.01μF	CE(2)	250V	22395

OS3350 DELAY EQUALISER & OUTPUT DRIVER (Cont.)

Ref	Value	Description	Tol %±	Part No
TRANSISTORS				
TR300		AE16		A31781
TR301		AE16		A31781
TR302		2N2369	I.T.T. Only	33701
TR303		2N2369	I.T.T. Only	33701
TR304		2N2369	I.T.T. Only	33701
TR305		2N2369	I.T.T. Only	33701
TR351		2N2369	I.T.T. Only	33701
TR352		2N2369	I.T.T. Only	33701
TR353		BD529		35840
TR354		BD529		35840
TR355		2N2369	I.T.T. Only	33701
TR356		2N2369	I.T.T. Only	33701
TR357		2N2369	I.T.T. Only	33701
DIODES				
D300	3V9	ZENER		33925
D351	3V3	ZENER		33923
MISCELLANEOUS				
L351	6.8μH			40451
L352	6.8μH			40451
L353		Ferrite FX1242		26986

| | | |

OS3550 TIMEBASE P.C.

Ref	Value	Description	Tol % ±	Part No	Ref	Value	Description	Tol % ±	Part No
RESISTORS									
R400	47	CF		28714	R455	3k3	CF		21803
R401	100k	CF	1W	19061	R456	1k5	CF		21801
R402	2k2	CF		21802	R457	100	CF		21794
R403	10	CF		21793	R458	5k6	CF		21806
R404	47	CF		28714	R459	10	CF		21793
R405	47	CF		28714	R460	10	CF		21793
R406	47	CF		28714	R461	330	CF		28721
R407	4k7	CF		21805	R462	33k	CF		21814
R408	1k5	CF		21801	R463	10	CF		21793
R409	10k	CF		21809	R464	10	CF		21793
R410	1k	CF		21799	R465	820	CF		28724
R411	3k9	CF		21804	R466	22k	CF		21812
R412	100	CF		21794	R467	470	CF		21797
R413	2k7	CF		28726	R468	220k	CF		21823
R414	220	CF		21796	R469	470	CF		21797
R415	1k5	CF	½W	18552	R470	390	CF		28722
R416	560	CF		21798	R471	4k7	CF		21805
R417	8k2	CF		21808	R472	2k7	CF		28726
R418	470k	CF		32330	R473	10	CF		21793
R419					R474	220	CF		21796
R420	10k	CF		21809	R475	1k	CF		21799
R421	220k	CF		21823	R476	1k5	CF	½W	18552
R422	33k	CF		21814	R477	91	MO		28782
R423	22k	CF		21812	R478	1k2	CF		21800
R424	1k8	CF		28725	R479	8k2	CF		21808
R425	33k	CF		21814	R480				
R426	1k	CF		21799	R481	180k	CF		21822
R427	1k	CF		21799	R482	1k2	CF		21800
R428	100k	CF		21819	R483	22k	CF		21812
R429	470	CF		21797	R484	4k7	CF		21805
R430	560k	CF		32359	R485	620	MO	5	22485
R431	100	CF		21794	R486	22k	CF		21812
R432	4k7	CF		21805	R487	1k8	CF		28725
R433	150k	CF		21821	R488	10	CF		21793
R434	3k9	CF		21804	R489	750	MO		28790
R435	39	CF		28713	R490	10	CF		21793
R436	47	CF		28714	R491	470	CF		21797
R437	12k	CF		21820	R492	4k7	CF		21805
R438	100	CF		21794	R493	820	CF		28724
R439	10	CF		21793	R494	100k	CF		21819
R440		Part of Switch, Trigger		34818	R495	1k5	CF		21801
R441	4k7	CF		21805	R496	10	CF		21793
R442	22	CF		28710	R497	10	CF		21793
R443	3k3	CF		21803	R498	120k	CF		21820
R444	4k7	CF		21805	R499	8k2	CF		21808
R445	1k5	CF		21801	R500	6k8	CF		21807
R446					R501	820	CF		28724
R447	100k	CF		21819	R502	100k	CF		21819
R448	27k	CF		21813	R503	8k2	CF		21808
R449					R504	3k3	CF		21803
R450	4k7	CF		21805	R505	1k2	CF		21800
R451	47	CF		28714	R506	4k7	CF		21805
R452	680	CF		28723	R507	10k			A4/34780
R453	1k	Control Pot. C.P.		26870	R508	4k7	CF		21805
R454	1k3	MO		28792	R509	1k2	CF		21800

OS3550 TIMEBASE P.C. (Cont.)

Ref	Value	Description	Tol % ±	Part No
RESISTORS (Cont.)				
R510	470	Control Pot. C.P.		28524
R511	10k	CF		21809
R512	3k3	MO		26726
R513	100	CF		21794
R514	3k3	MO		26726
R515	100	CF		21794
R523	100	CF		21794
R524	47k	CF		21815
R525	6k8	CF		21807
R526	470	CF		21797
R527	100	CF		21794
R530	10k	CF		21809
R531				
R532	390	CF	½W	18545
R533	6k8	CF		21807
R534	1k	CF		21799
R535	4k7	CF		21805
R536	1k	CF		21799
R537	10	CF		21793
R538	10M	CC		1179
R539	47	CF		28714
R540	4k7	CF		21805
R541	10k	CF		21809
R542	6k8	CF		21807
R543	4k7	CF		21805
R544	1k3	CC		33338
R545	100	CF		21794
R546	47	CF		28714
R547	47	CF		28714
R548	100k	CF		21819
R549	2k7	CF		28726
R550	10	CF		21793
R551	390	CF		28722
R552	100k	CF		21819
R553	2k	MO		26731
R554	680	CF		28723
R555	1k	CF		21799
R556	1k8	CF		28725
R557	33	CF		28712
R558	47	CF		28714
R559	100	CF		21794
R560	47k	CF		21815
R561				
R562				
R563				
R564				
R565		Shown on Interconnect		
R566		Circuit Drawing		
R567				
R568				
R569				
R570				
R571	22	CF		28710

Ref	Value	Description	Tol % ±	Part No
R572				
R573	15	CF		28708
R574	3k9	CF		21804
R575				
R576	100	CF		21794
R577	470	CF		21797
R578		A.O.T.		
R579	15	CF		28708
CAPACITORS				
C400	47pF	SM		4502
C401	220pF	CE(2)		22379
C402	.47μF	PE	160V	31381
C403	470pF	CE(2)		22383
C404	33pF	CE(2)		22370
C405	100pF	CE(2)		22376
C406	10pF	CE(2)		22364
C407	33pF	CE(2)		22370
C408	47pF	CE(2)		22372
C409	.01μF	CE(2)		22395
C410	1000pF	CE(2)		22387
C411	.1μF	CE(1)	160V	31377
C412	.1μF	CE(1)	160V	31377
C413	100pF	CE(2)		22376
C414	1000pF	CE(2)		22387
C415	220pF	CE(2)		22379
C416				
C417	.1μF	CE(2)		19647
C418	.1μF	CE(2)	160V	31377
C419	.01μF	CE(2)		22395
C420	22pF	CE(2)		22368
C421	.1μF	CE(1)		19647
C422	.1μF	CE(1)		19647
C423	1000pF	CE(2)		22387
C424	390pF	CE(2)		22382
C425	22μF	E	25V	32181
C426	27pF	CE(2)		22369
C427	.01μF	CE(2)		22395
C428	.01μF	CE(2)		22395
C429	1.5pF	SM		813
C430	22pF	CE(2)		22368
C431	18pF	CE(2)		22367
C432	6.8pF	CE(2)		22362
C433	.01μF	CE(2)		22395
C434	.01μF	CE(2)		22395
C435	6/25pF	TRIMMER		23593
C438	100pF	CE(2)		22376
C439	.01μF	CE(2)		22395
C440	33pF	CE(2)		22370
C444	.01μF	CE(2)		22395
C445				
C446	.1μF	CE(1)		19647
C447	220pF	CE(2)		22379

OS3550 TIMEBASE P.C. (Cont.)

Ref	Value	Description	Tol % ±	Part No
CAPACITORS (Cont.)				
C448	.01μF	CE(2)		22395
C449	.01μF	CE(2)		22395
C450	.01μF	CE(2)		22395
C451	.01μF	CE(2)		22395
C452	33μF	E	16V	32175
C453	.01μF	CE(2)		22395
C454	1000pF	CE(2)		22387
C455	22pF	CE(2)		22368
C456		Shown on Interconnect Circuit Drawing		
C457				
C458				
C459				
C460				
C461				
C462	.01μF	CE(2)		22395
C463	4.7pF	CE(2)		29649
C464				
C465	27pF	CE(2)		22369
C466	1500pF	CE(2)		22388
C467	.01μF	CE(2)		22395
TRANSISTORS				
TR401		BSX20		23307
TR402		BSX20		23307
TR403		BC107		26790
TR404		2N3906		21533
TR405		BC107		26790
TR406		2N3906		21533
TR407		BC108		26110
TR408				
TR409		2N930		21548
TR410		2N3906		21533
TR411		2N3906		21533
TR412		BC107		26790
TR413		AE13 Matched Pair		A31254
TR414				
TR415		MPS3640		24128
TR416		MPS3640		24128
TR417		BSX20		23307
TR418		BC108		26110
TR419		BSX20		23307
TR420		BSX20		23307
TR421		2N3906		21533
TR422		2N3906		21533
TR423		2N930		21548
TR424		BC108		26110
TR425		AE31 Matched Pair		A36243
TR426				
TR427		BC107		26790
TR428		2N3906		21533
TR429		AE13 Matched Pair with TR436		A31254
TR430		2N3906		21533
TR431		MPS3640		24128
TR432		2N3906		21533
TR433		C407		20388
TR434		MPS3640		24128
TR435		BSX20		23307
TR436		See TR429		
TR437		BSX20		23307
TR438		BSX20		23307
DIODES				
D401		1N4148	Selected	34701
D402		1N4148		23802
D403		1N4148		23802
D404		1N4148		23802
D405		1N4148		23802
D406		1N4148		23802
D407		1N4148		23802
D408		1N4148		23802
D409		1N4148		23802
D410		1N4148		23802
D411		1N4148		23802
D412		1N4148		23802
D413				
D414		0A47		4468
D415		0A47		4468
D416		1N4148		23802
D417		1N4148		23802
D418		1N4148		23802
D419		AAZ13		4472
D420		1N4148	Selected	34701
D421		1N4148		23802
D422		1N4148	Selected	34701
D423		ZENER 6.8V		4666
D424		1N4148		23802
D425		0A47		4468
D426		1N4148		23802
D427				
D428		1N4148	Selected	34701
D429		1N3595		29330
D430				
D431		1N4148	Selected	34701
D432		1N4148		23802
D433		1N4148		23802
D434				
D435		1N4148		23802
D436		1N4148		23802
D437				
D438		1N4148		23802
D439		1N4148		23802
MISCELLANEOUS				
L402		Bead Ferrite FX1242		26986
S40				34818
S41			Part of R440	
S42				A3/35756
SKE		50Ω BNC		1222

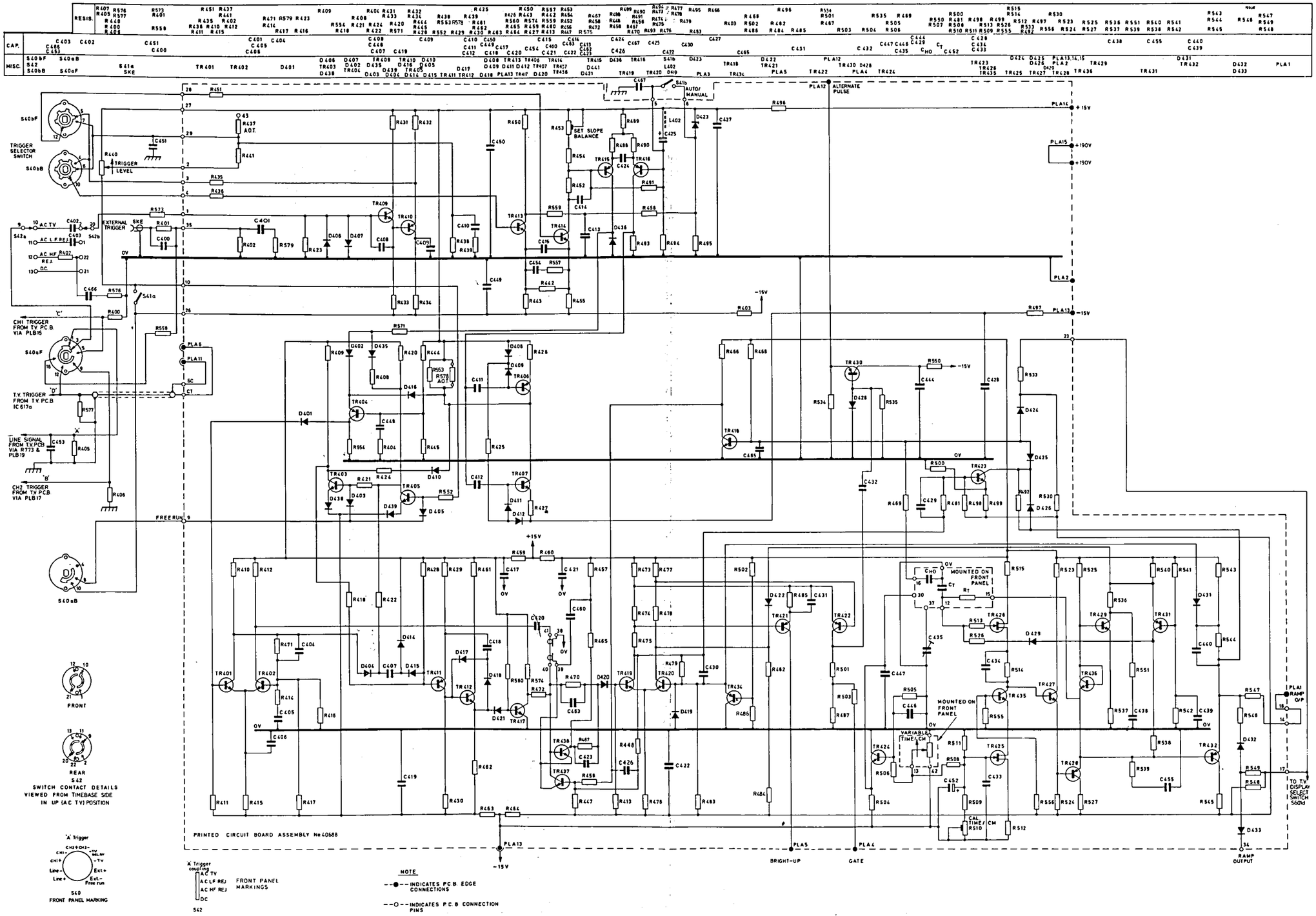


Fig. 5 Circuit Diagram Timebase

OS3350 T.V. LOGIC

Ref	Value	Description		Tol % ±	Part No
RESISTORS					
R600 }					
R601					
R602					
R603					
R604					
R605					
R606 }				See SK2598	
R607					
R608					
R609					
R610					
R611 }					
R612	220	CF			21796
R613	1k5	CF			21801
R614					
R615	3k3	CF			21803
R616	680	CF			28723
R617	100	PCP			40496
R618	390	MF		2	38584
R619	10M	CF			32661
R620	430	MF		2	38583
R621	47	CF			28714
R622	68	CF			28716
R623	47	CF			28714
R624	1k3	MF		2	38597
R625	2k7	CF	A.O.T.		38726
R626	820μF	MF		2	38592
R627	1k	MF		2	38594
R628	18k	CF	A.O.T.		38624
R629	5k1	MF		2	38611
R630	68	CF			28716
R631	47μF	CF			28714
R632	220	MF		2	38578
R633	750	MF		2	38591
R634					
R635	75	MF			40710
R636	101μF	CF			21809
R637	100k	CF			21819
R638	3k9	MF		2	38608
R639	2k	MF		2	38601
R640	11k	MF		2	38619
R641	10k	CF			21809
R642	10k	CF			21809
R643	10k	CF			21809
R644	1k8	MF		2	38600
R645	100	CF			21794
R646	120	WW		2.5W	40502
R647	560	CF			21798
R648	3k	MF		2	38605
R649	4k7	MF		2	38610
R650	820	MF		2	38592
R651	3k	MF		2	38605
R652	1k	CF			21799
R653	2k7	CF			28726
R654	100	CF			21794
R655	100	CF			21794
R656	5k6	CF			21806
R657	330k	MF		2	38654
R658	5k1	MF		2	38611
R659	2k7	MF		2	38604
R660	1M	MF		2	40493
R661	1M8	MG			35752
R662	330	CF			28721
R663	56k	CF			28729
R664	5k6	CF			21806
R665	56k	MF		2	38636
R666	3k3	CF			21803
R667	4k7	CF			21805
R668	18k	MF		2	38624
R669	100	CF			21794
R670	5k6	CF			21806
R671	6k8	CF			21807
R672	100k	CF			21819
R673	10k	CF			21809
R674	75	MF	A.O.T.	2	38567
R675	1k	MF		2	38594
R676	820	MF		2	38592
R677	1k2	MF		2	38596
R678	1k	CF			21799
R679	560	MF			21798
R680	1k	CF			21799
R681	2k2	MF			21802
R682	2k2	MF			21802
R683	4k7	CF			21805
R684	10	CF			21793
R685					
R686	3k3	CF			21803
R687	1k5	CF			21801
R688	2k2	CF			21802
R689	2k2	CF			21802
R690	220	CF			21796
R691	240	MF		2	38579
R692	10k	CF			21809
R693	39k	CF			28728
R694	1k	CF			21799
R695	3k3	CF			21803
R696	330	CF			28721
R697	10k	CF			21809
R698	1k	CP	Coarse }	X Shift }	35294
R699	1k	CP	Fine }	Control }	
R700	30k	MF		2	38629
R701	20k	MF		2	38625
R706	6k8	MF		2	38614
R707	220	MF		2	26743
R708	430	MF		2	38585
R709	22k	CF			21812
R710	22k	CF			21812
R711	10k	CF			21809
R712	10k	CF			21809

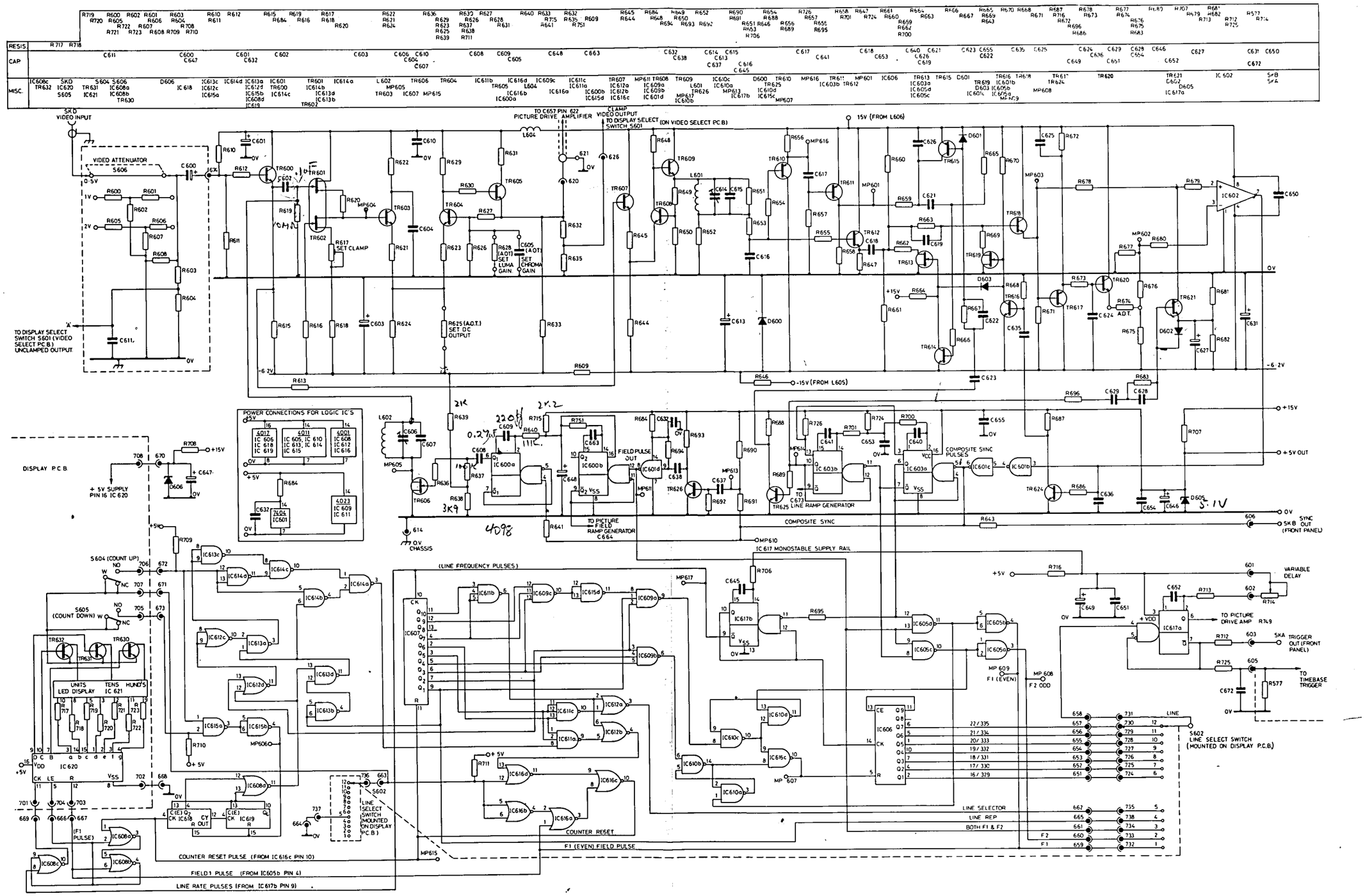


Fig. 6A Circuit Diagram TV Logic SK2604 Issue 1

OS3350 T.V. LOGIC (Contd.)

Ref	Value	Description		Tol % ±	Part No
RESISTORS (Cont.)					
R713	3k6	MF	2		38607
R714	100k	CP			A4/40701
R715	2k2	CF			21802
R716	2k2	CF			21802
R717	470	CF			21797
R718	470	CF			21797
R719	470	CF			21797
R720	470	CF			21797
R721	470	CF			21797
R722	470	CF			21797
R723	470	CF			21797
R724	10	CF			21793
R725	6k8	CF			21807
R726	10k	CF			21809
R730	160k	MF	2		38647
R731	15k	MF	2		38622
R732	1k2	CF			21800
R733	680	MF	2		38590
R734	56	CF			28715
R735	6k2	MF			38613
R736	820	CF		¼W	28724
R737	10	CF			21793
R738	4k7	CF			21805
R739	20k	MF	2		38625
R740					
R741	680	CF			28723
R742	5k6	WW		2.5W	40720
R743	6k8	WW		2.5W	40721
R744	100	CF			21794
R745	1k5	CF			21801
R746	3k9	CF			21804
R747	1k6	CF			38599
R748	47k	MF	5		21815
R749	4k7	CF			21805
R750	1k	CF			21799
R751	30k	MF	2		38629
R752	10M	CF			32661
R753	470k	MF	2		38658
R754	10M	CF	A.O.T. 10		32661
R755	100k	CF			21819
R756	5k6	MF	5		21806
R757	330	CF			28721
R758	75k	MF	2		38639
R759	68k	CF	A.O.T.		21816
R760	220k	CF			21823
R761	5k6	CF			21806
R762	36k	MF	2		38631
R763	18k	MF	2		38624
R764	15k	MF	2		38622
R765	5k6	CF			21806
R766	100k	CF			21819
R767	2k7	MF	5		28726
R768					
R769	33k	CF			21814

Ref	Value	Description		Tol % ±	Part No
R773	470	CF			21797
R774	33k	CF			21814
R775	3k3	CF			21803
R776	4k3	MF	2		38609
R777	750	MF	½		40528
R778	250	MF	2		40529
R779	2k0	MF	2		38601
R780	2k0	MF	2		38601
R781	1k	PCP			40495
R782	1k5	MF	2		38598
R783	8k2	MF	2		38616
R784	10k	MF	2		38618
R785	470	CF			21797
R786	1k	PCP			40495
R787	4k7	MF	2		38610
R788	10	CF			21793
R789	47	CF			28714
R790	200k	MF	2		38649
R791	150k	MF	2		38646
R792	47k	MF	2		38634
R793	1M	MF	2		40493
R794	13k	MF	2		38621
R795	2k0	MF	2		38601
R796	5k6	MF	2		38612
R797	2k2	CF			21802
R798	3k6	MF	2		38607
CAPACITORS					
C600		See SK2598			
C601	22µF	T		20V	40462
C602	.1µF	CE(1)		50V	40466
C603	22µF	T		16V	54220
C604	.047µF	CE(1)		25V	40464
C605	5.6pF	CE(2) A.O.T.			22361
C606	45pF	TRIMMER			36274
C607	360pF	PF A.O.T.	2	125V	40719
C608	.27µF	CE(1)		50V	40467
C609	220pF	PF	2	125V	40477
C610	.1µF	CE(1)		25V	36709
C611		See SK2598			
C612					
C613	22µF	T		16V	54220
C614	45pF	TRIMMER			36274
C615	100pF	PF	2	125V	37206
C616	100pF	PF	2	125V	37206
C617	.1µF	CE(1)		50V	40466
C618	.1µF	CE(1)		50V	40466
C619	.1µF	CE(1)		50V	40466
C620					
C621	150pF	PF	2	125V	40476
C622	1000pF	CE(2)			22387
C623	.047µF	CE(1)		25V	40464
C624	.1µF	CE(1)		50V	40466
C625	.27µF	CE(1)		50V	40467
C626	330pF	PF	2	125V	40479

OS3350 T.V. LOGIC (Cont.)

Ref	Value	Description	Tol % ±	Part No
CAPACITORS (Cont.)				
C627	22μF	T	16V	54220
C628	1000pF	CE(2)		22387
C629	.047μF	CE(1)	25V	40464
C630	1μF	T	35V	54221
C631	1μF	T	35V	54221
C632	.047μF	CE(1)	25V	40464
C633				
C634				
C635	270pF	PF	2 125V	40478
C636	100pF	PF	2 125V	37206
C637	3600pF	PF	2 63V	40484
C638	5600pF	PF	2 63V	40486
C639				
C640	4700pF	PF	2 63V	40485
C641	680pF	PF	2 125V	40481
C645	430pF	PF	2 125V	40480
C646	22μF	T	16V	54220
C647	33μF	T	10V	40463
C648	33μF	T	10V	40463
C649	33μF	T	10V	40463
C650	.01μF	CE(2)		22395
C651	.1μF	CE(1)	50V	40466
C652	1000pF	PF	2 63V	35918
C653	.01μF	CE(2)		22395
C654	.1μF	CE(1)		40466
C655	470pF	CE(2)		22383
C656	330pF	CE(2)		22381
C657	6.8μF	T	35V	40461
C658	330pF	PF	2 125V	40479
C659	3.3μF	T	35V	40460
C660	15μF	T	20V	40483
C661	6.8μF	T	35V	40461
C662				
C663	.01μF	CE(1)	50V	40465
C664	.1μF	CE(1)	50V	40466
C665	.33μF	CE(1)	10 50V	40469
C666	6.8μF	T	35V	40461
C667	6.8μF	T	35V	40461
C668	6.8μF	T	35V	40461
C669	.01μF	CE(2)		22395
C670	6.8μF	T	35V	40461
C671	.1μF	CE(1)		40466
C672	150pF	CE(2)		22378
C673	.047μF	CE(1)	25V	40464
C674	6200pF	PF	2 63V	40487
C675	1μF	T	35V	54221
C676				
C677	.33μF	CE(1)	10 50V	40469
C678	.01μF	CE(2)		22395
C679	22μF	T	16V	54220
C680	.01μF	CE(2)		22395
C681				
C682	10pF	PF	2 125V	40471
C683	8.2pF	PF		40470

Ref	Value	Description	Tol % ±	Part No
C684	45pF	TRIMMER		36274
C685	.01μF	CE(2)		22395
C686	.01μF	CE(2)		22395
C687	.01μF	CE(2)		22395
LAMPS				
L601	10μH			40491
L602	3.3μH			40490
L603	100μH			40492
L604	100μH			40492
L605	3.3μH			40490
L606	3.3μH			40490
TRANSISTORS				
TR600		2N2369		23307
TR601, TR602		DUAL FET AE31		A36243
TR603		2N2369		23307
TR604		2N2369		23307
TR605		2N2369		23307
TR606		BF244		36354
TR607		BC109		29236
TR608		BC109		29236
TR609		BC109		29236
TR610		BCY71		40497
TR611		BCY71		40497
TR612		BC109		29236
TR613		E112 or TIS75		40499
TR614		2N2369		23307
TR615		BCY71		40497
TR616		BC109		29236
TR617		BCY71		40497
TR618		BC109		29236
TR619		E112 or TIS75		40499
TR620		BC109		29236
TR621		BC109		29236
TR622				
TR623				
TR624		BC109		29236
TR625		2N2369		23307
TR626		BC109		29236
TR627				
TR628				
TR629				
TR630		2N2369		23307
TR631		2N2369		23307
TR632		2N2369		23307
TR633		BC109		29236
TR634		BC109		29236
TR635		2N2369		23307
TR636		BC109		29236
TR637		BCY70		70182
TR638		BCY70		70182
TR639		BC109		29236
TR640		BC109		29236

OS3350 T.V. LOGIC (Contd.)

Ref	Value	Description	Tol % ±	Part No
TRANSISTORS (Cont.)				
TR641		BC109		29236
TR642				
TR643				
TR644		BC108		26110
TR645		BC108		26110
TR646		2N3906		21533
TR647		2N930		21548
TR648		2N3906		21533
DIODES				
D600	6.2V	ZENER	5	33930
D601		1N4148		23802
D602		1N4148		23802
D603		1N4148		23802
D604				
D605	5.1V	ZENER	5	33928
D606	5.1V	ZENER	5	33928
D607				
D608				
D609		1N4148		23802
D610	24V	ZENER	5	33944
D611		1N4148		23802
D612		1N4148		23802
D613		1N4148		23802
D614		1N4148		23802
D615		1N4148		23802
D616	6.5V	BZX91 Zener	5 .005%oc TC	40722
D617				
D618		1N3595		29330
D619		1N4148		23802
D620	10V	ZENER	5	33935

Ref	Value	Description	Tol % ±	Part No
INTEGRATED CIRCUITS				
IC600		4098		40509
IC601		7404		31836
IC602		TL710 CP		40494
IC603		96L02		40510
IC604				
IC605		4011		34953
IC606		4017		37689
IC607		4040		40506
IC608		4001		36195
IC609		4023		37812
IC610		4011		34953
IC611		4023		37812
IC612		4001		36195
IC613		4011		34953
IC614		4011		34953
IC615		4011		34953
IC616		4001		36195
IC617		4098		40509
IC618		4017		37689
IC619		4017		37689
IC620		74C925		40513
IC621	5082-7433	LED Display		40504
SWITCHES				
S601		Display Select Switch (3 way wafer)		A4/40711
S602		Line Select Switch (12 way wafer)		A4/40712
S603		Push button 8125ZM3		40700
S604		Push button 8125C		40512
S605		Push button 8125C		40512

RESIS	R730 R731 R760 R733 R735 R736 R737 R749 R738 R750 R748 R739 R753 R756 R757 R754 R796 R798 R755 R741 R742 R744 R747 R780 R776 R782 R785 R779 R786 R789 R788 R762 R759 R761 R680 R734 R765 R752 R758 R790 R791 R752 R793 R794 R795 R797 R769 R767 R777 R778 R766 R763 R696 R745 R699 R698 R781 R783 R784 R787 R773
CAPS	C657 C673 C658 C674 C659 C664 C670 C675 C661 C660 C665 C656 C683 C667 C684 C668 C671 C682 C669 C680 C685 C677 C686 C679 C678 C687
MISC	TR633 TR634 TR638 TR639 TR635 TR640 TR636 D613 MP612 D409 D630 TR637 D614 TR641 TR647 D618 D615 D619 TR648 S43 S601 S603 SKE SKC L603 D610 TR644 TR645 D612 L605 L606 D616 TR646

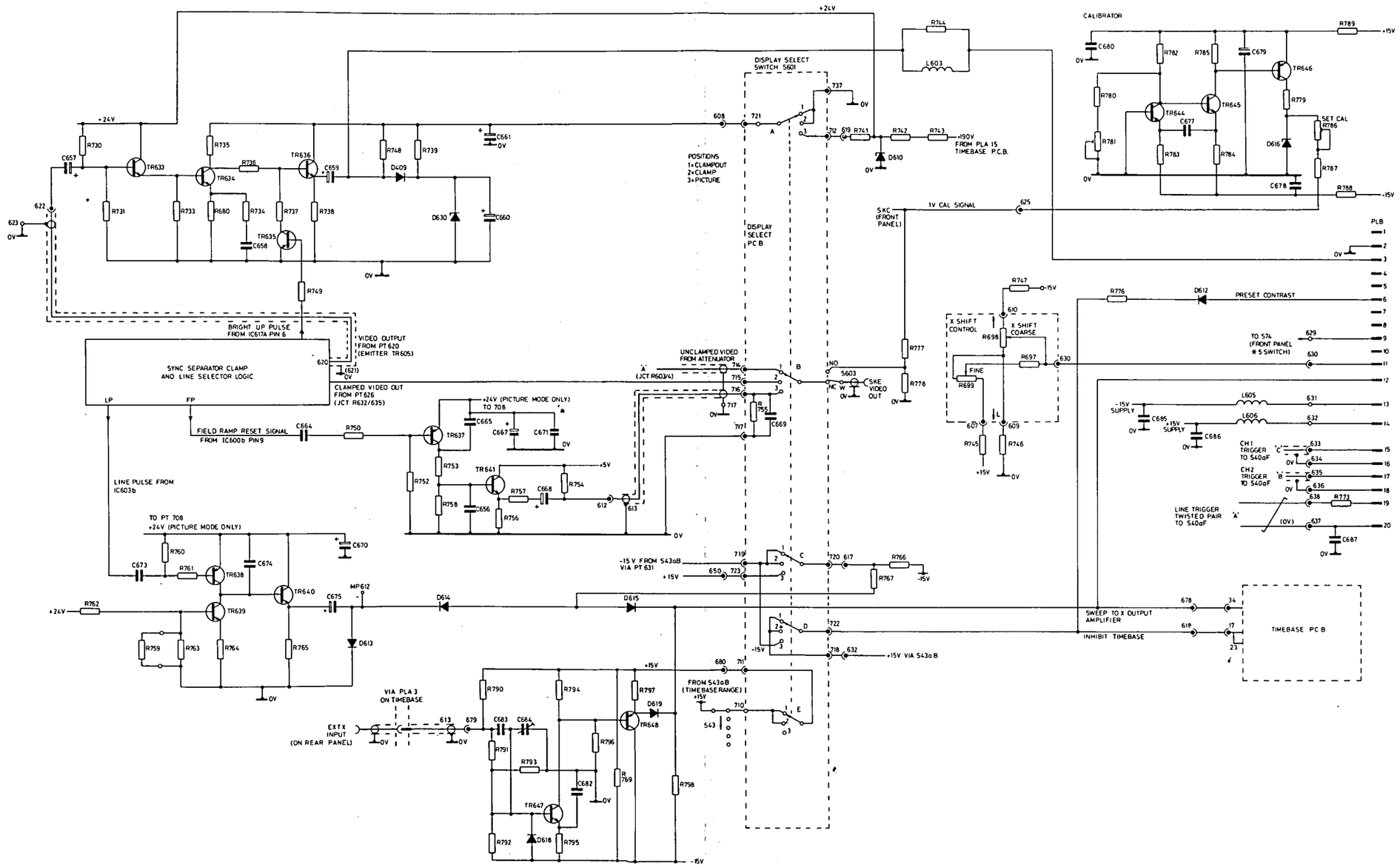


Fig. 6B Circuit Diagram TV Logic SK2604 Issue 1

OS3350 'X' O/P BRIGHT-UP INTERCONNECTION P.C.B.

Ref	Value	Description		Tol % ±	Part No
RESISTORS					
R900	10	CF			21793
R901	33	CF			28712
R902	33	CF			28712
R903	47k	CF			21815
R904	68k	CF			21816
R905	47k	CF			21815
R906	330	CF			28721
R907	4k7	MO			26722
R908	3k9	CF			21804
R909	Sk1	MO			28794
R910	680	CF			28723
R911	100	CF			21794
R912	47k	CF			21815
R913	22k	CF			18566
R914	47k	CF			21815
R915	10k	CF			21809
R916	39k	CF			29
R917	100	CF			21794
R918	2k2	CF			18554
R919	47k	CF			21815
R920	68k	CF			21816
R921	10k	CF			21809
R922	100	CF			21794
R923	47k	MF			38634
R924	47k	CF			21815
R925	150	CF			28719
R926	2k2	CF			21802
R927	820	MF	A.O.T.	2	38592
R928	750	MF		2	38591
R929	100	CF			21794
R930	680	CF			28723
R931	3k9	CF			21804
R932	390	CF			28722
R933	470	CF			21797
R934	56k	CF			28729
R935	10k	CP			40444
R936	220	CP			40445
R937	560	CF			21798
R938	470	CF		5	21797
R939	100	CF			21794
R940	750	MF		2	38591
R941	330	CF			28721
R942	150	CF			28719
R943	47k	MF		2	38634
R944	47k	CF			21815
R945	1k5	CF			21801
R946	100	CF			21794
R947	10	CF			21793
R948	100	CF		6	21794
R949	10	CF			21793
R950	10k	CF			21809
R951	6k8	CF			21807
R952	1k5	CF			21801
R953	47k	CF			21815
R954	10M	CF			32661
R955	10k	CF			21809
R956	180k	CF			21822
R957	1k5	CF			21801
R958	1k	CF			21799
R961	270	CF			28720
R962	270	CF			28720
R963	100	CF			21794
R970	4k7	CF			21805
R971	2k4	MF		2	38603
R972	47	CF			28714
R973	3k9	CF			21804
R974	5k6	CF			21806
R975	1k8	CF			29725
R976	100	CF			21794
R977	39k	MF			38632
R978	82k	MF			38640
R979	3k9	CF			21804
R980	22k	MO		1W	41483
R981	10	CF			21793
R982	47k	CF			21815
R983	10	CF			21793
R984	10	CF			21793
R985	470	CF			21797
R986	10	CF			21793
R987	15M	MO			40446
R988	1M	CP			40443
R989	1M	CF			31840
R990	10k	CF			21809
R991	100k	CF			21819
R992	10k	CF			21809
R993	68k	MF			38638
R994	47	CF			28714
R995				A.O.T.	
CAPACITORS					
C901	.01μF	CE(2)		250V	22395
C902	47μF	E		25V	32182
C903	.01μF	CE(2)		250V	22395
C904	.01μF	CE(2)		250V	22395
C905	.1μF	PE		16V	31377
C906	.01μF	CE(2)		250V	22395
C907	5.6pF	CE(2)			22361
C908	.1μF			100V	37018
C909	.01μF	CE(2)		250V	22395
C910	.1μF			100V	37018
C921	.01μF	CE(2)		250V	22395
C922	.01μF	CE(2)		250V	22395
C923	.01μF	CE(2)		250V	22395
C924					
C925	100pF	CE(2)			22376
C926	.1μF	PE		160V	31377
C927	.01μF	CE(2)			22395

OS3350 'X' O/P BRIGHT-UP INTERCONNECTION P.C.B. (Cont.)

Ref	Value	Description	Tol %±	Part No
CAPACITORS				
C928	100pF	CE(2)	500V	22376
C929			A.O.T.	
C930	120pF			22377
C931	.01μF	CE(2)	250V	22395
C932			A.O.T.	
C970	.01μF	CE(2)	250V	22395
C973	2.7pF	CE(2)		816
C974	820pF	CE(2)		22386
C975	.01μF	CE(2)	250V	22395
C976	.1μF	PE	160V	31377
C978	.01μF	CE(2)	2.5kV	40450
C979	.01μF	CE(2)	2.5kV	40450
C980	2200pF	CE(2)	500V	22389
C981	.01μF	CE(2)	2.5kV	40450
C982	.01μF	CE(2)	250V	22395
C983	.01μF	CE(2)	250V	22395
C984	.01μF	CE(2)	250V	22395
C985			A.O.T.	
TRANSISTORS				
TR901		BC107		26790
TR902		2N3906		21533
TR903		BC108		26110
TR904		BC182B		33205
TR905		BC182B		33205
TR921		BC182B		33205
TR922		BC182B		33205
TR923		MPSU04		38723
TR924		BF470		38416
TR925		2N2369		23307
TR926		BF470		38416
TR927		MPSU04		38723
TR928		BC182B		33205
TR929		BC182B		33205

Ref	Value	Description	Tol %±	Part No
TR970		2N2369		23307
TR971		BC450/BC448/MPS8599		40128
TR972		BC449		40129
DIODES				
D901		1N4148		23802
D902		1N4148		23802
D903		1N4148		23802
D904		1N4148		23802
D905		1N4148		23802
D921		1N4148		23802
D922	4V7	ZENER		33927
D923		1N4148		23802
D924		1N4148		23802
D925		1N4148		23802
D926	3V3	ZENER		33923
D927	6V8	ZENER		33931
D928		1N4148		23802
D970		1N4148		23802
D971		1N4148		23802
D972		1N4148		23802
D973		1N4148		23802
D974		1N4149		1949
D975		1N4149		1949
D976		1N4148		23802
MISCELLANEOUS				
RL921				35357
L970		Ferrite FX1242		26986
N971				26845
N972				26845
SKA				31240
SJB				31241
SKC				31241

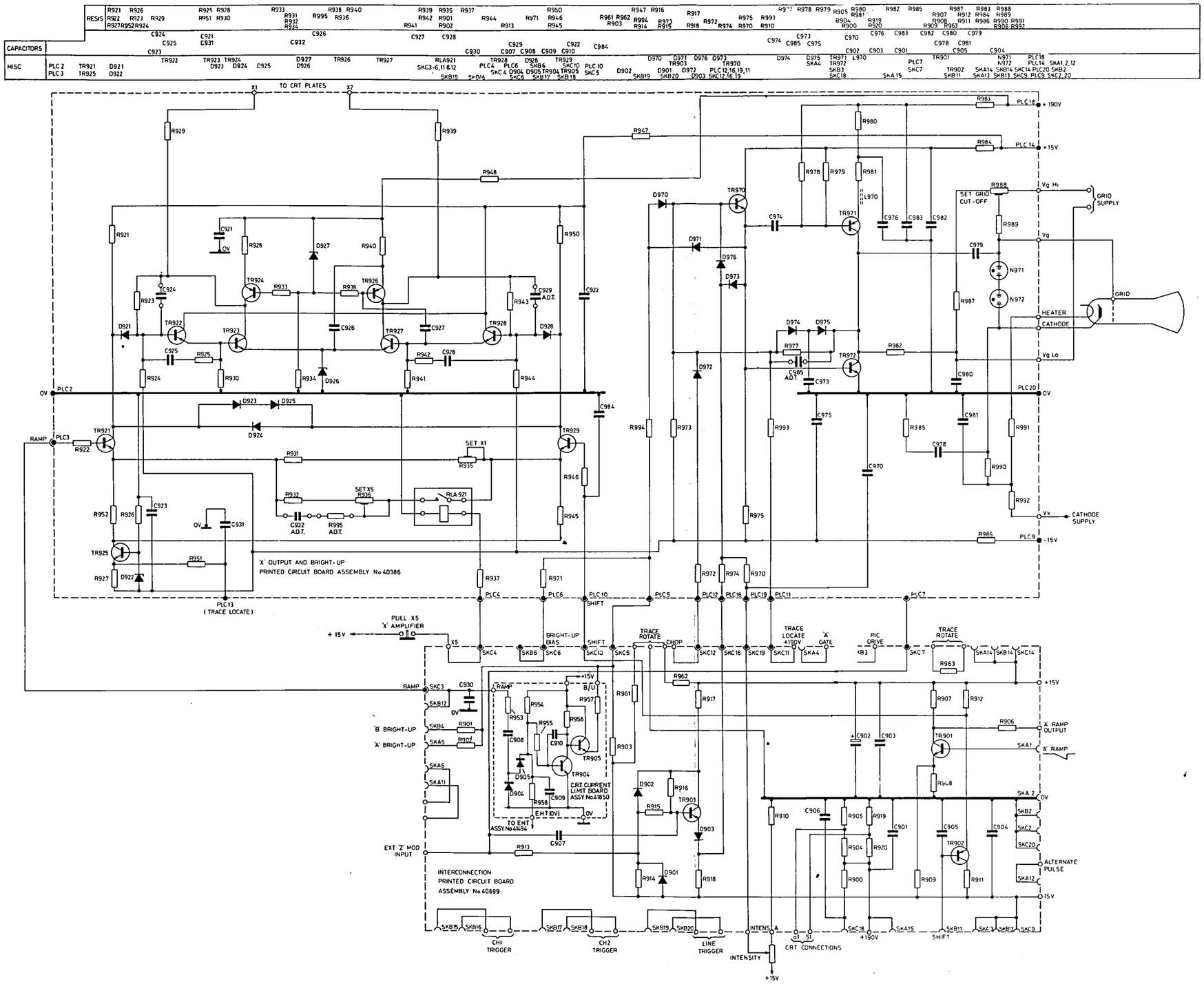


Fig. 7 Circuit Diagram 'X' Output, Bright-up & Interconnection SK2602 Issue 1

OS3350 POWER SUPPLY & EHT OSCILLATOR

Ref	Value	Description	Tol %±	Part No
RESISTORS				
R83	68k	CF		21816
R84	47	WW	5	18739
R85				
R86	4k7	CF		21805
R802	1M2	MG		33589
R803	2M7	MG		40448
R804	10k	CF		21809
R805	15M	MG		40446
R806	220	CF		21796
R807	1k5	CF		21801
R808	5k6	CF		21806
R809	3k3	CF		21803
R810	1k	CF		21799
R811	68k	CF		21816
R812	6k8	CF		21807
R813	120	CF		28718
R814	1k3	MF	2	38597
R815	1k	CF		21799
R816	22k	CF		21802
R817	10	CF		21793
R831	22	CF	1W	19028
R832	470	CF		21797
R833	180	CF		21795
R834	3k3	CF		21803
R835	OR82	WW	2½W	31889
R836	OR82	WW	2½W	31889
R837	7k5	MO	2	28797
R838	1k	PCP		26870
R839	6k8	MO	2	28796
R840	820	CF		28724
R841	2k7	CF	1W	19043
R842	100k	MO	2	28822
R843	3k6	MO	2	26725
R844	4k7	CF		21805
R845	1k	CF		21799
R846	4k7	CF		21805
R847	7k5	MO	2	28797
R848	7k5	MO	2	28797
R852	1k2	CF		21800
R853				
R854	47k	PCP		28335
R855	3k3	CF		21803
R856	100	CF		21794
R857	22k	CF		21812
R858	91	MO	2	28821
R862	1	WW	3W	31890
R866	47	WW		18739
CAPACITORS				
C83	100µF + 200µF	E	275V	24740

Ref	Value	Description	Tol %±	Part No
C84	4700µF	E	40V	31919
C85	4700µF	E	40V	31919
C86	100µF + 200µF	E	275V	24740
C87	.22µF	PE	400V	31396
C88	4.7µF	PE	63V	32195
C801	4700pF		4kV	26863
C802	4700pF		4kV	26863
C803	4700pF		4kV	26863
C804	500pF		8kV	26862
C805	500pF		8kV	26862
C806	0.1µF		25V	36709
C807	68µF	T	25V	54337
C808	.33µF		160V	35603
C809	150pF	CE(2)	500V	22378
C810	.01µF	CE(2)	250V	22395
C811	100µF	T	6V3	35714
C812	0.1µF		25V	36709
C831	10µF	E	25V	32180
C832	100pF	CE(2)	500V	22376
C833	.01µF	CE(2)	250V	22395
C834	3000pF	CE(2)	500V	22391
C835	10µF	E	25V	32180
C836	.01µF	CE(2)	250V	22395
C837	.01µF	CE(2)	250V	22395
C838				
C839	22µF	E	25V	32181
C840				
C841	10µF	E	25V	32180
TRANSISTORS				
TR801		2SC1173		36188
TR802		BC212		29327
TR803		BC212		29327
TR804		BC182B		33205
TR805		2N5831		20388
TR831		BC212K		29327
TR832		BSX20		23307
TR833		BC108		26110
TR834		BC108		26110
TR835		MM1614		19320
TR836		2N3053		4039
TR837		MJE520		24739
TR838		MJE520		24739
TR839		2N5296		28630
TR843		MJE520		24739
DIODES				
D83		1N4003		32771
D84		1N4003		32771
D85		1N4007		52337
D86		1N4007		52337

OS3350 POWER SUPPLY & EHT OSCILLATOR (Cont.)

Ref	Value	Description	Tol % ±	Part No
DIODES (Cont.)				
D87	56V	ZENER		35760
D801	120V	ZENER		40633
D802		BY187		31817
D803		BY187		31817
D804		BY187		31817
D805		1N4148		23802
D806		BY187		31817
D807		1N4148		23802
D808		1N4148		23802
D809		1N4148		23802
D810		1N4148		23802
D831		1N4148		23802
D832		1N4148		23802
D833		1N4148		23802
D834		1N4148		23802
D835		1N4003		23462
D836		1N4003		23462
MISCELLANEOUS				
IC801		μA723C		31228
L801	150μH			35826
L802		Ferrite FX1242		26986
T83				A1/40058
T801				A2/40095
N80				26586
FS83		For 110V 1A Slo-Blo		34790
FS83		For 240V 0.5A Slo-Blo		33685
FS831		250mA		32338
FS832		500mA		32339
FS833		1A		52162
FS834		1A		52162
S80		With R60		A4/31224
S81				35242
MR81		W04		29367
MR82		1N4003 4 off per		32771
MR83		W02		19725

| | | |

OS3350 INTERCONNECTIONS

Ref	Value	Description	Tol % ±	Part No
RESISTORS				
R26	250		With S12	A4/31257
R27	250		With R37	A4/40453
R28	39	CF		28713
R29	39	CF		28713
R30	39	CF		28713
R31	39	CF		28713
R32	180	CF		21795
R33	180	CF		21795
R34	1M	CF		31840
R35	39	CF		28713
R36	39	CF		28713
R37	250		With R27	A4/40453
R38	1k	CF		21799
R60	4k7		Part of S80	A4/31224
R80	470k			A4/31222
R81	100k			A4/35941
R82	4k7			A4/31223
R85	8k2	WW		19802
R561				
R562				
R563				
R564				
R565		Resistor Module		A3/36454
R566				
R567				
R568				
R569				
R570				
R575	1k	CF		21799
R600	24R9	MF	0.5	40523
R601	24R9	MF	0.5	40523
R602	100	MF	0.5	40524
R603	75	MF	0.5	40525
R604	75	MF	0.5	40525
R605	44R9	MF	0.5 Non-Pref-	40527
R606	44R9	MF	0.5erred Value	40527
R607	40R2	MF	0.5	40522
R608	150	MF	0.5	40526
R609	10	CF		21793
R610	43k	MF	2	38633
R611	7k5	MF	2	38615

Ref	Value	Description	Tol % ±	Part No
CAPACITORS				
C23	1.5pF	SM		813
C456	68pF	SM		34353
C457	1μF		1 160V	24888
C458	0.1μF		1 160V	24887
C459	0.01μF		1 160V	24886
C460	900pF		1 125V	24885
C461	100pF	CE(2)		22376
C600	220μF	E	10V	32169
C611	39pF	PF A.O.T.	2 125V	37204
DIODES				
D441	LED			35202
MISCELLANEOUS				
V83		Thorn D14–310GH		40658
L83				A3/35997
LP1	12V			36634
LP2	12V			36634
S12			With R26	A4/31257
S31				40455
S43				31280
S51				35502
S74				31280
S76		With R698/699		35294
S201				40693
S606				A3/40695
SKA				24159
SKB				24159
SKC				24159
SKD				1222
SKE				1222

DRAWING No.		
SK2598	RES'S	R608 R603 R604 R600 R507 R602 R601 R575 R568 R567 R569 R565 R566 R570 R564 R563 R607 R605 R777 R778 R561 R562 R714 R28 R29 R32 R33 R60 R30 R31 R34 R85 R80 R81 R82
FIRST USED ON 053350	C611	C600 C456 C458 C457 C459 C460 C461 C23
	CAP	
	MISC	S606 SKD D441 SKE S74 S43aF S43bB S603 SKC S31bF S43bF S43bB SKA SKB S76 S31aB S43cB S43cF S12 SKY-1 S51b SK2 S201 V83 S51a LP1 LP2 L83 PLD

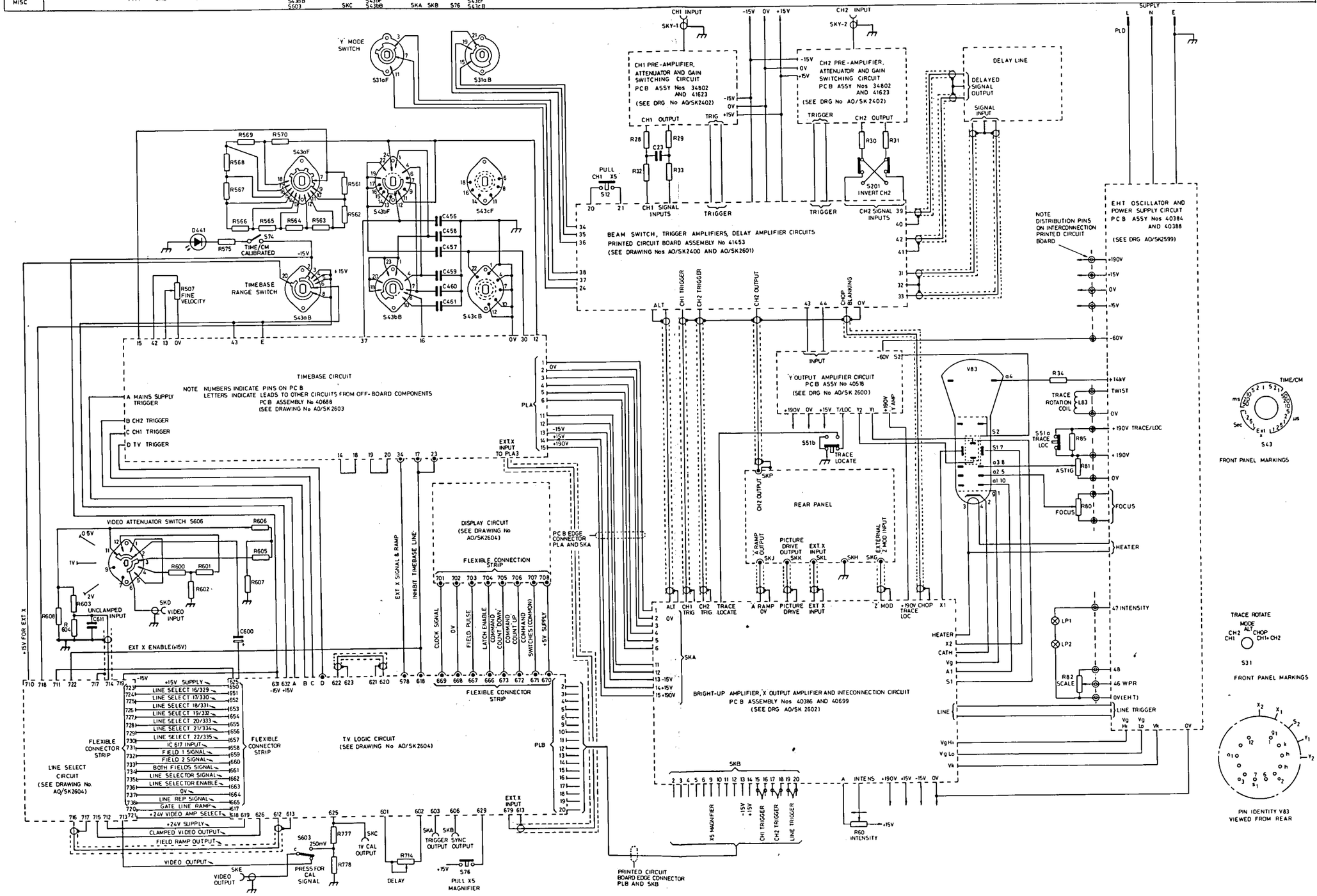


Fig. 9 Circuit Diagram Interconnections SK2598 Issue 1

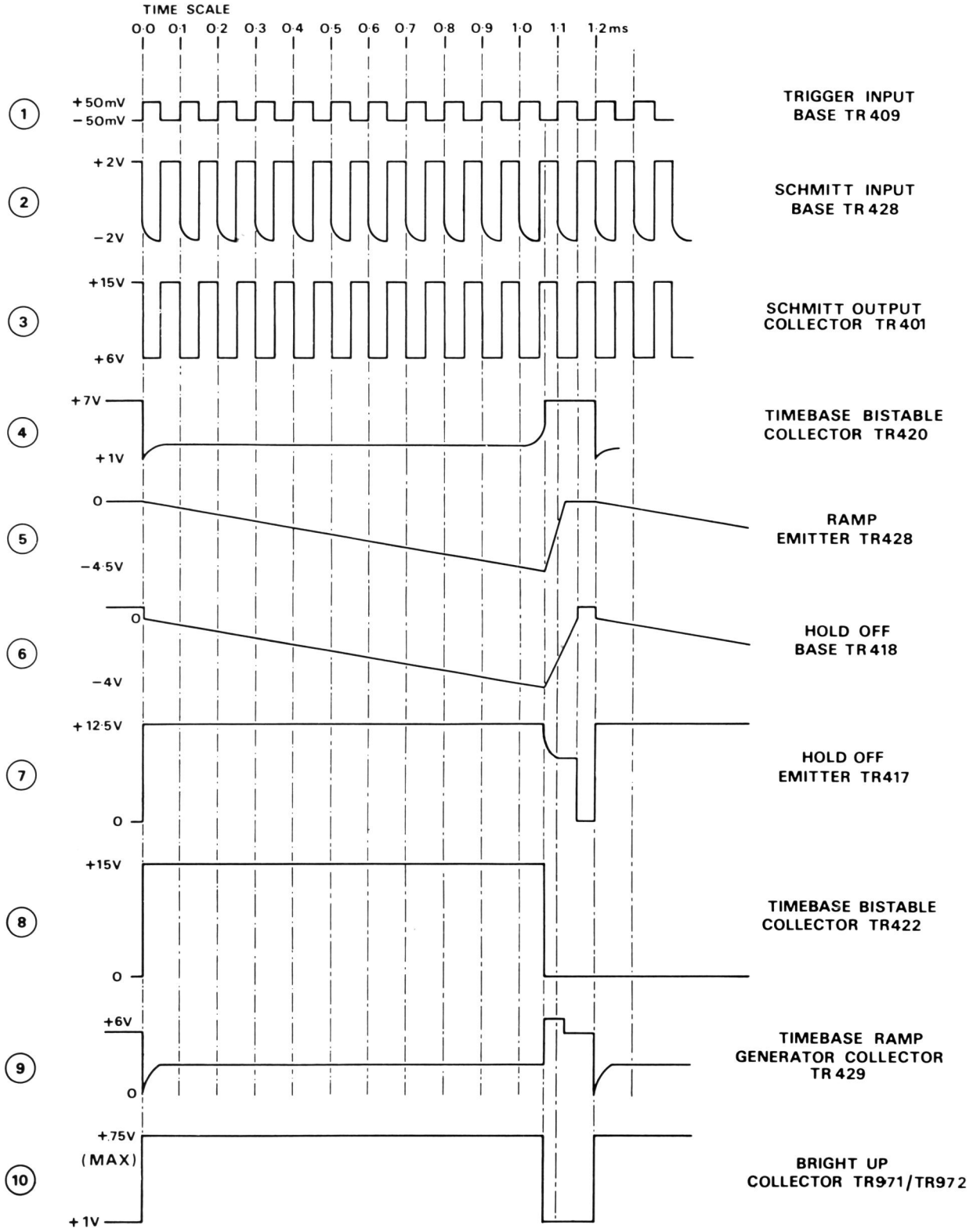


Fig. 10 Waveform Diagram Normal Sweep

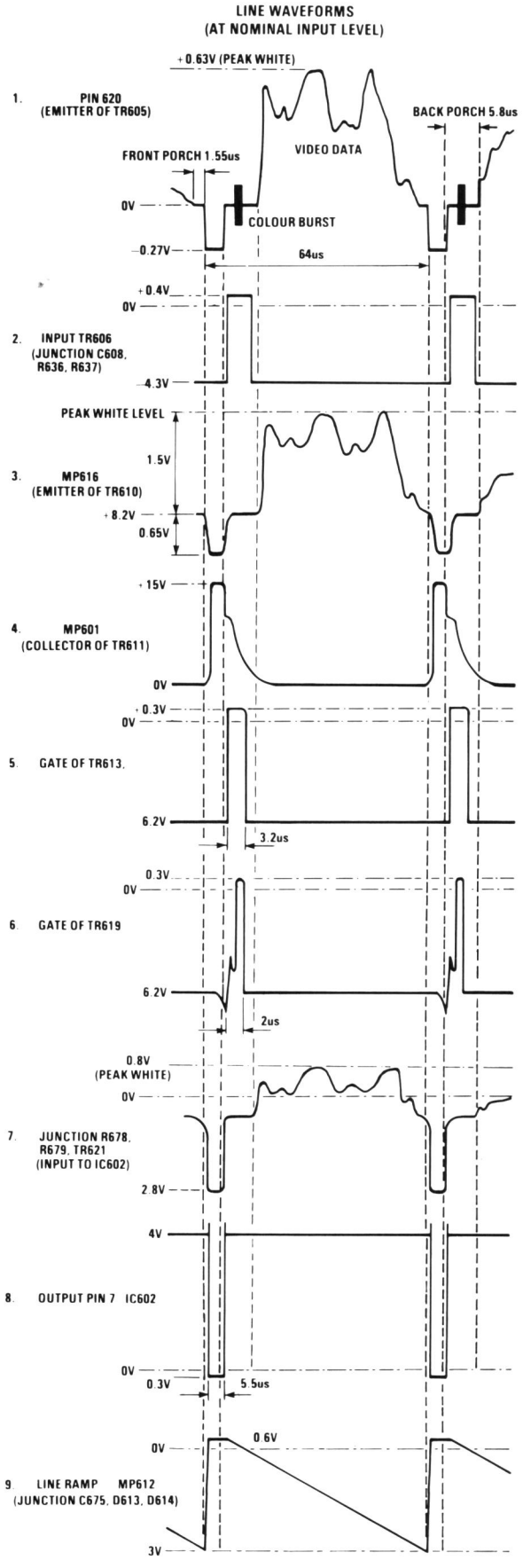


Fig. 11 TV Waveform

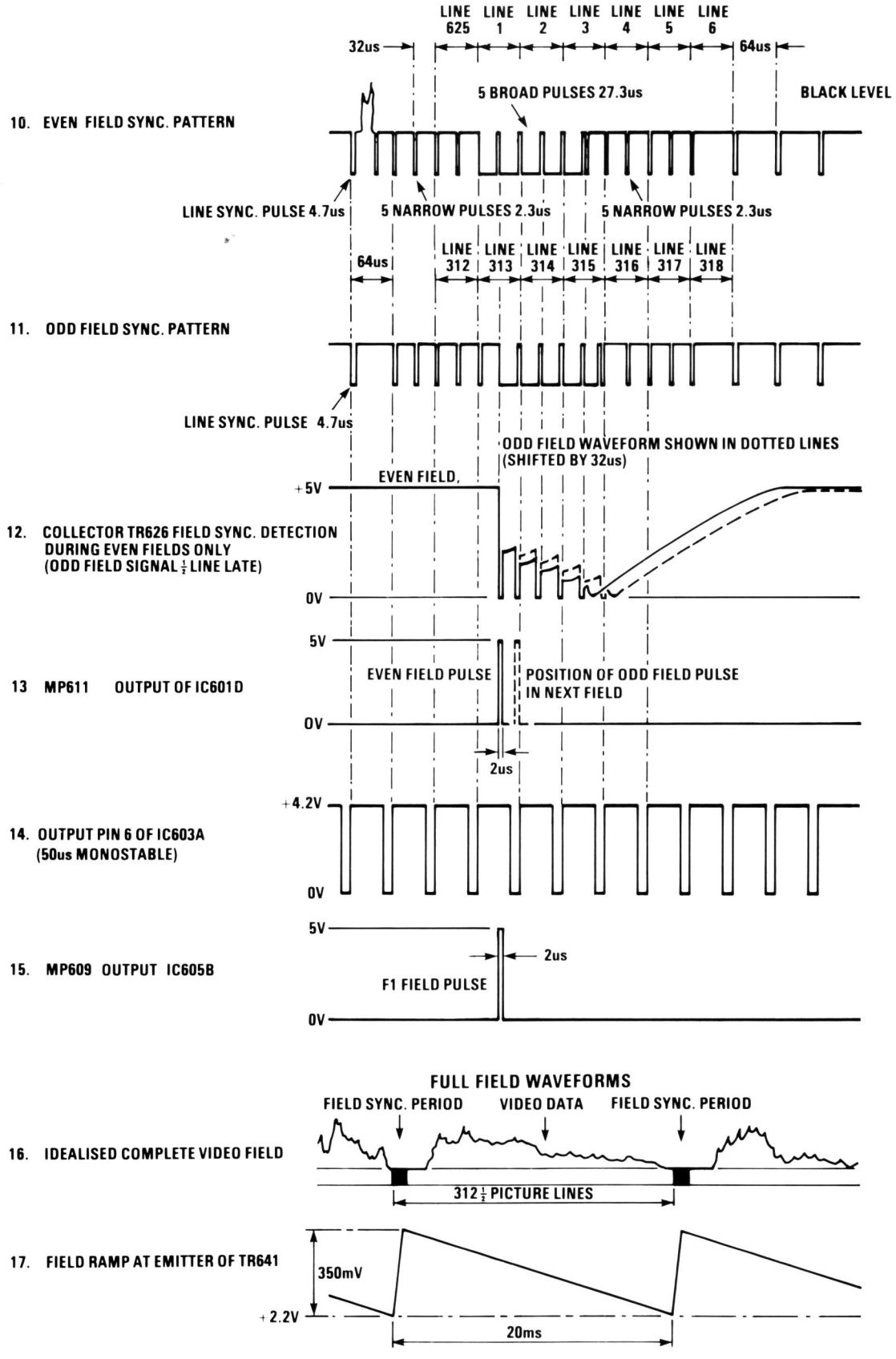


Fig. 12 Field Synch Period Waveforms

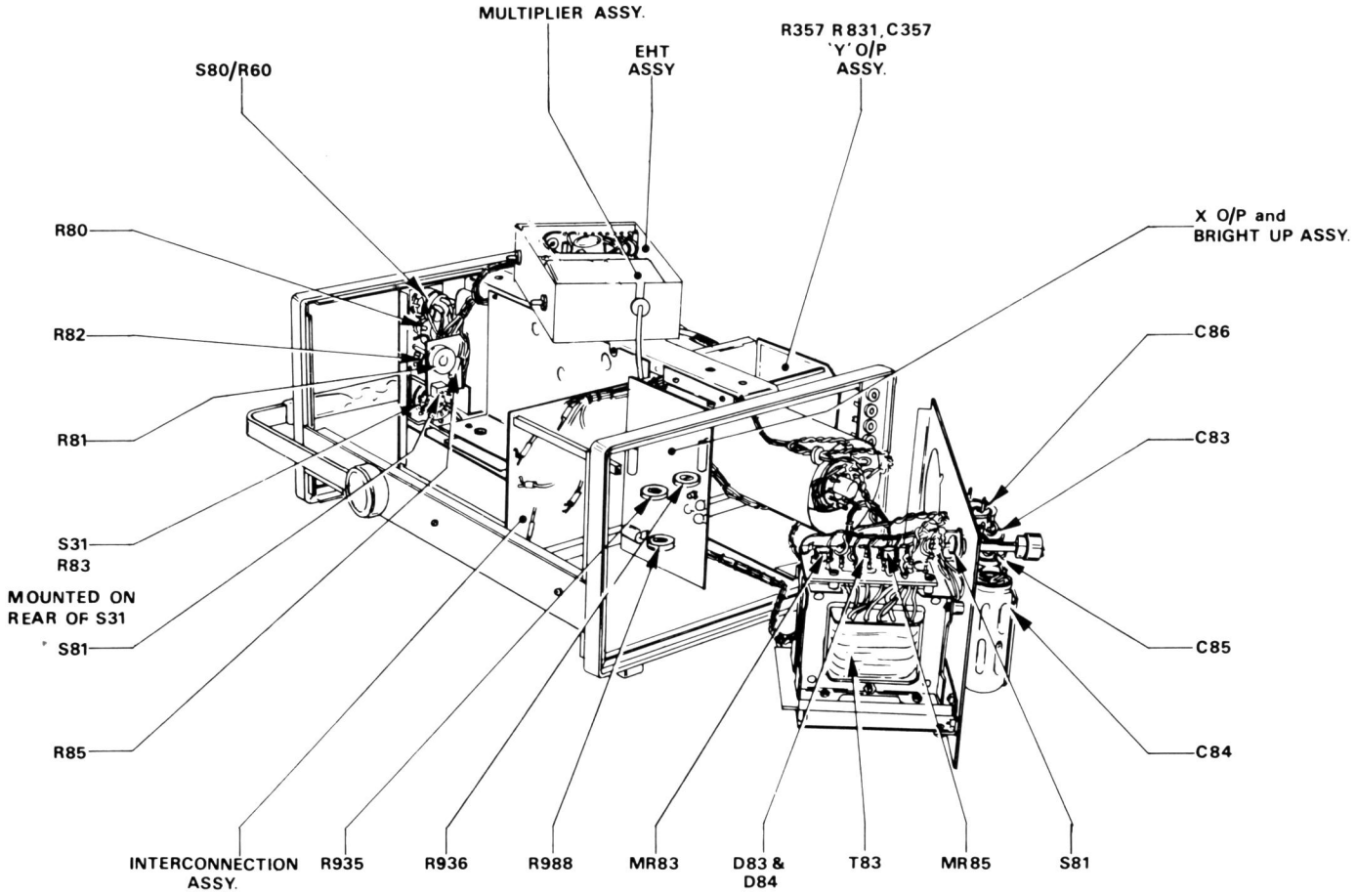


Fig. 13 Main Frame showing access

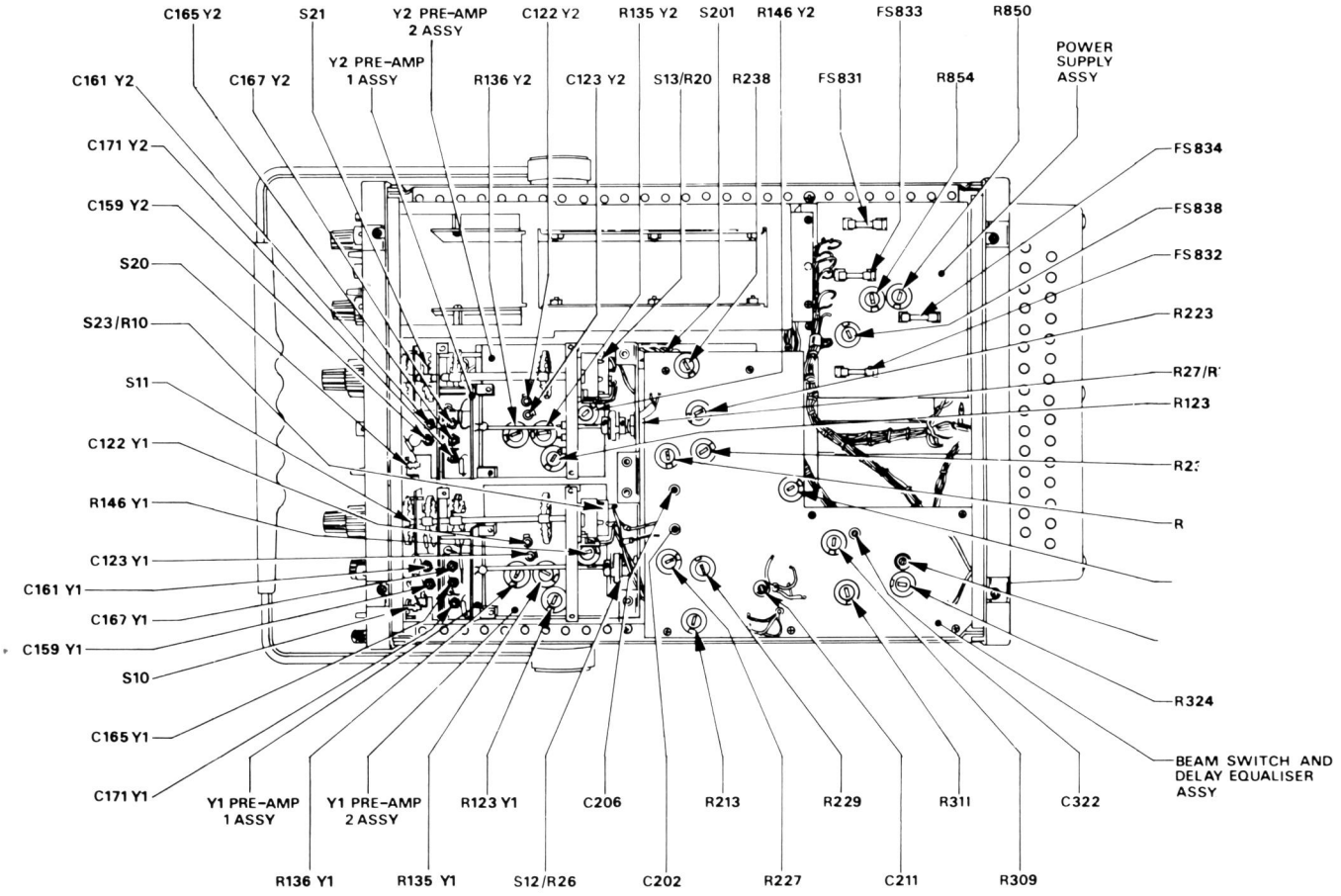


Fig. 14 Underside view

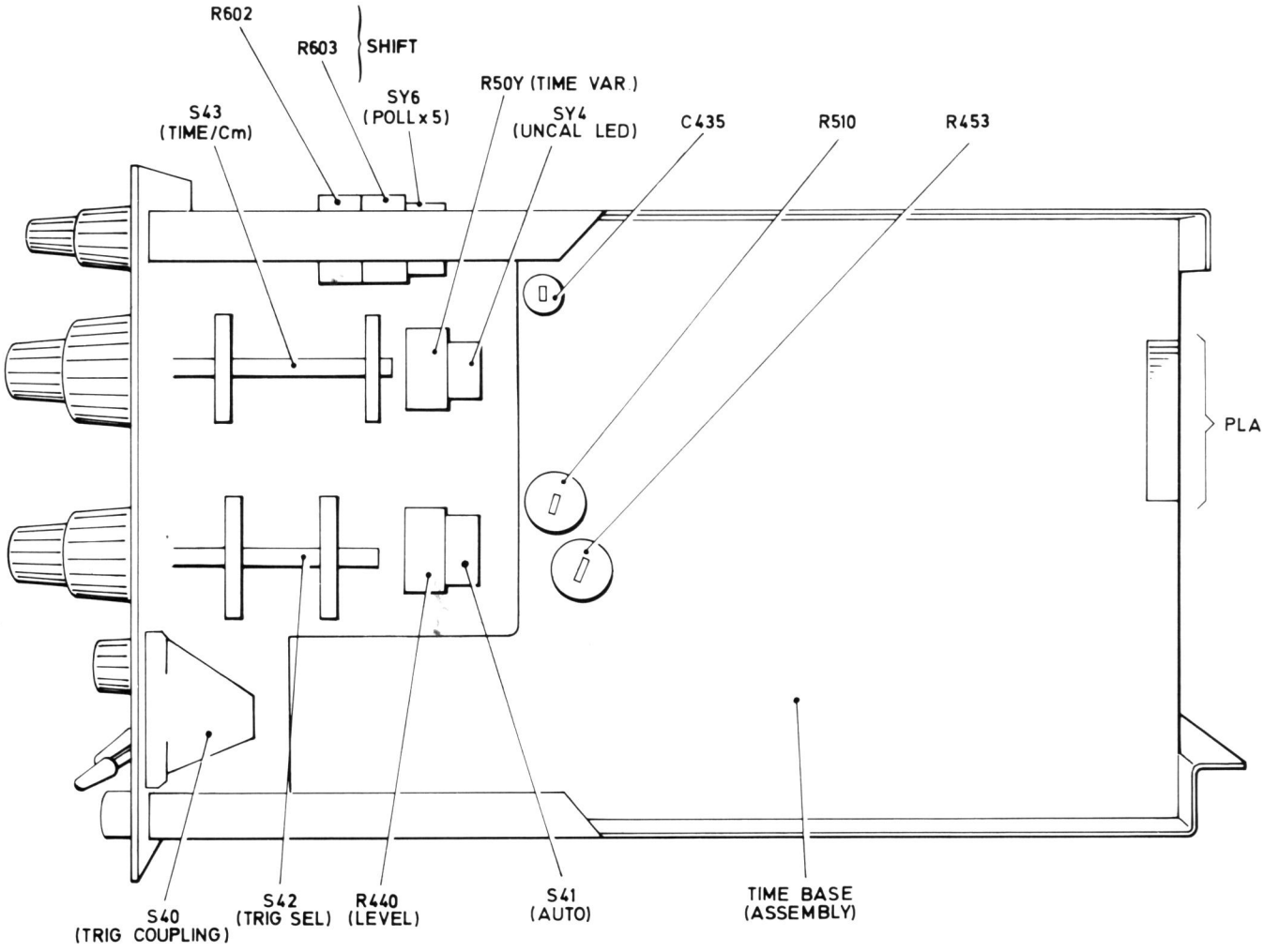


Fig. 15 Timebase unit right hand view